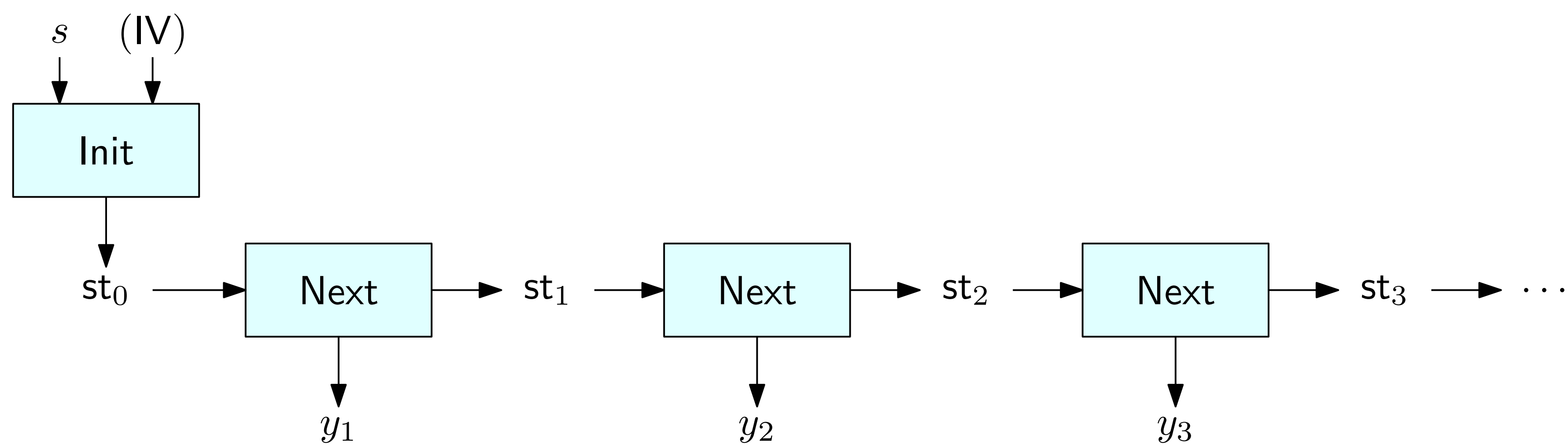
Stream ciphers (reminder)

A stream cipher is a pair of deterministic polynomial-time algorithms

- **Init:** takes a n-bit seed s, and possibly a n-bit *initialization vector* (IV), and outputs a *state* st
- **Next:** takes a state st and outputs a bit y and a new (updated) state st′

Idea: we can generate as many random bits as desired, by repeatedly calling Next



* In practice, **Next** can output multiple bits at once (e.g., a byte)

Stream ciphers (reminder)

If the stream cipher does not support IVs, then it should behave like a PRG

- For a key chosen u.a.r., its output should be indistinguishable (to poly-time adversaries) from a uniform stream of random bits chosen independently at random (as long as the output length is polynomial)

If the stream cipher does support IVs, then the stream cipher should behave like a PRF

- For any key (chosen u.a.r.) the output streams generated from multiple IVs (chosen u.a.r.) should be indistinguishable (to poly-time adversaries) from multiple streams of random bits, where each bit is chosen u.a.r.

- This must still be true even if the adversary is given the IVs!

Stream ciphers (reminder)

- We don't know if (secure) stream ciphers exist (we don't know if PRGs / PRFs exist)
- In practice we have some candidate stream cipher constructions that are conjectured to be secure
- These construction have withstood years of public scrutiny and attempted cryptanalysis

- Some popular practical constructions of stream ciphers:
  - Trivium: optimized for hardware
  - RC4 (insecure): optimized for software
  - ChaCha20: replacement of RC4

Trivium

- Stream cipher selected as part of the eSTREAM portfolio

European project to "identify new stream ciphers suitable for widespread adoption"

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- Designed to be easy to implement in hardware
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- Based on feedback shift registers (FSR)

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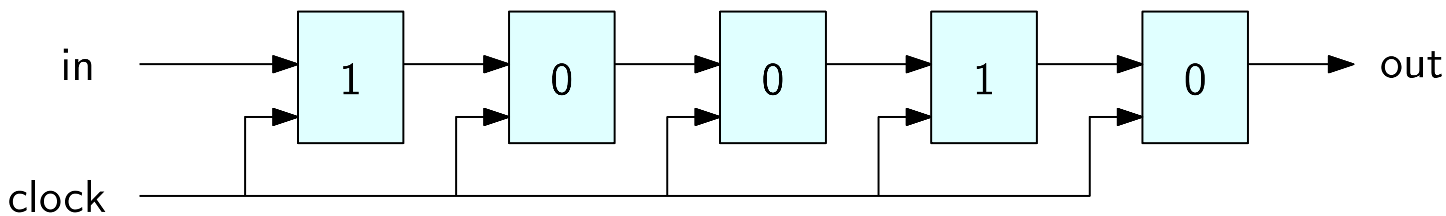
- Based on feedback shift registers (FSR)

Shift Registers

- Shift register with n bits



Shift Registers

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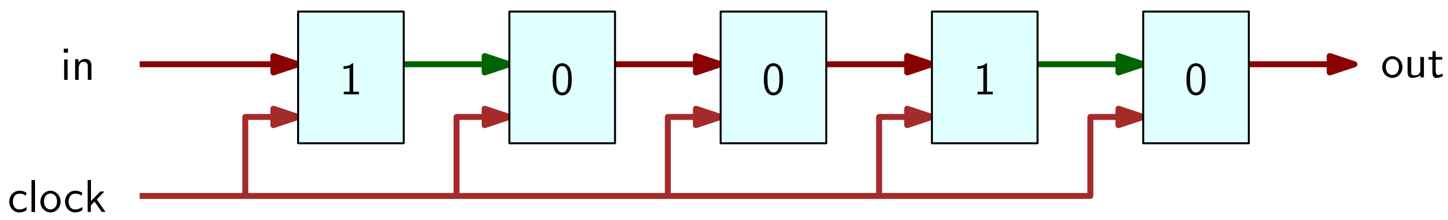
- The stored bits update (their values shift to the right) at each clock tick



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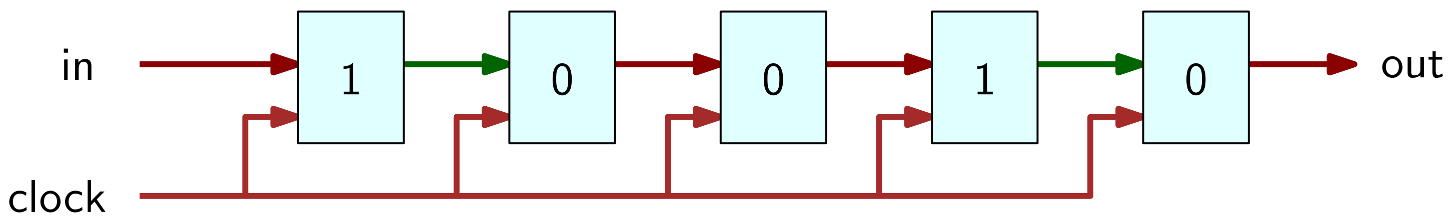

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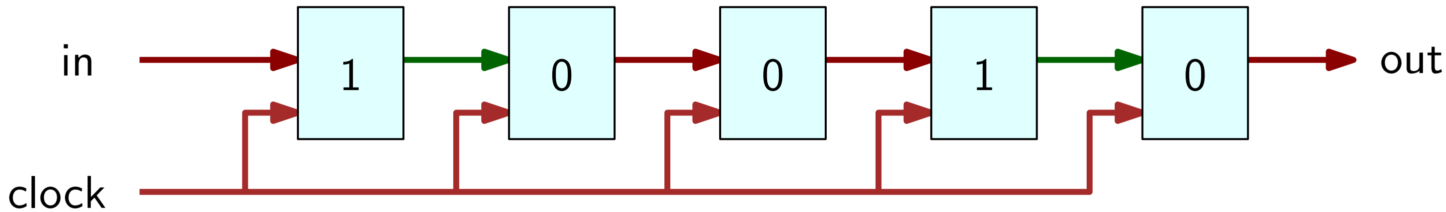

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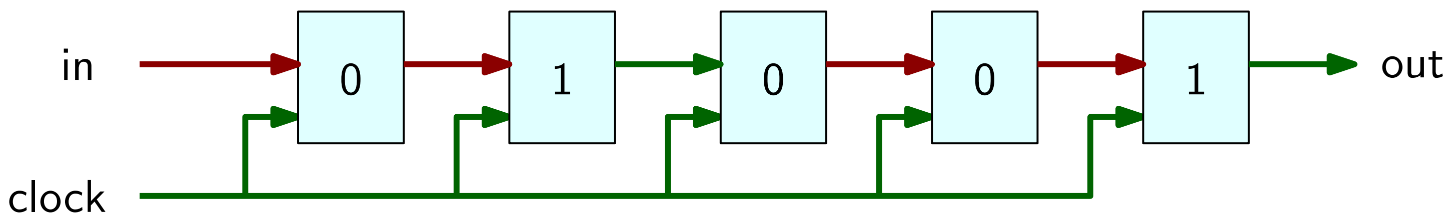

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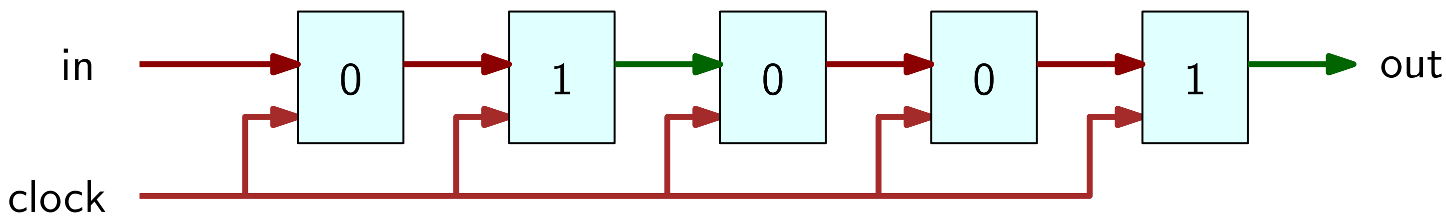

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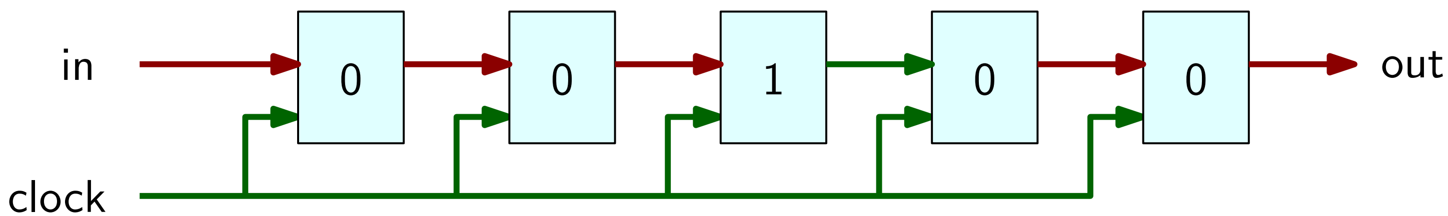

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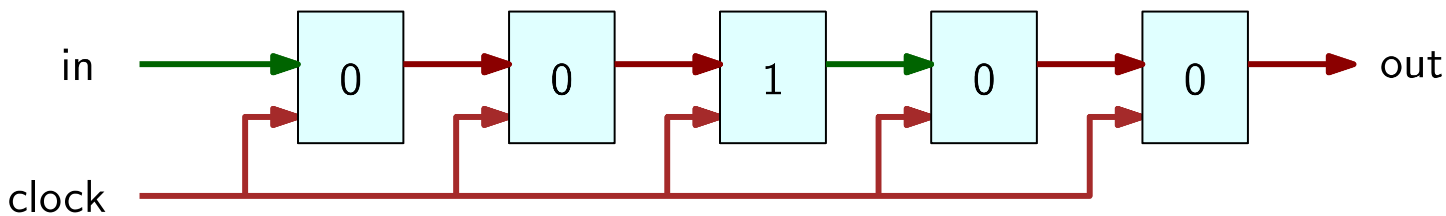

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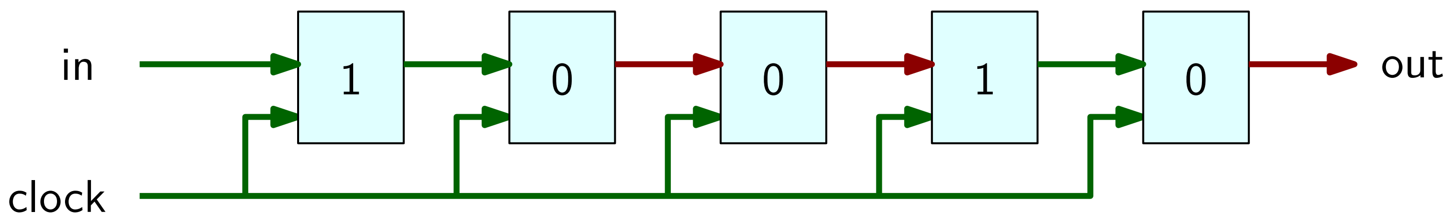

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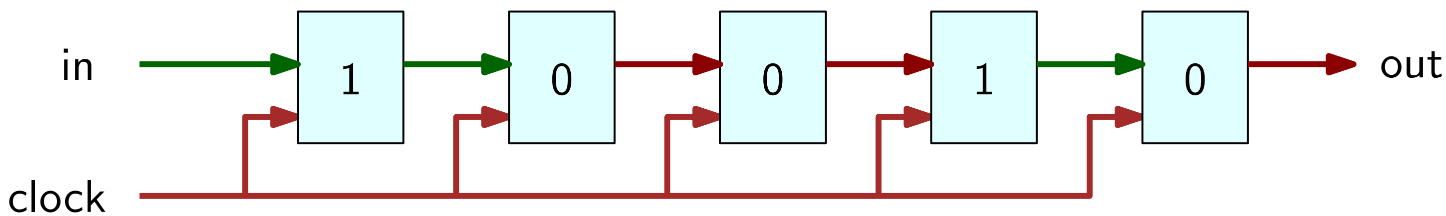

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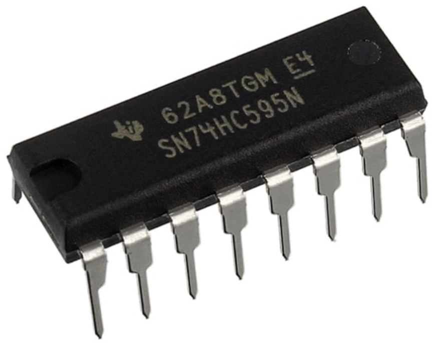

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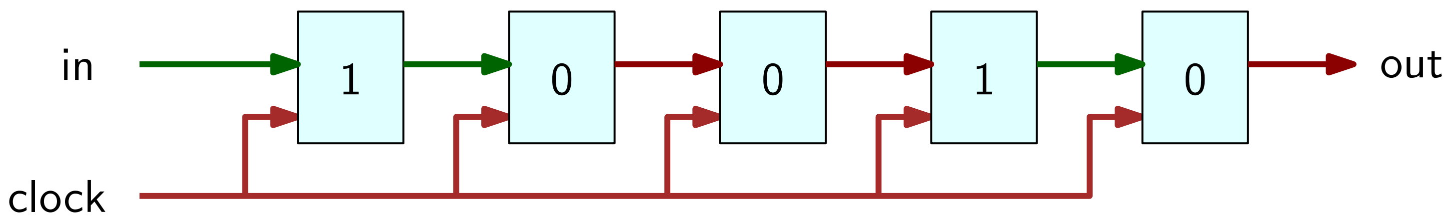

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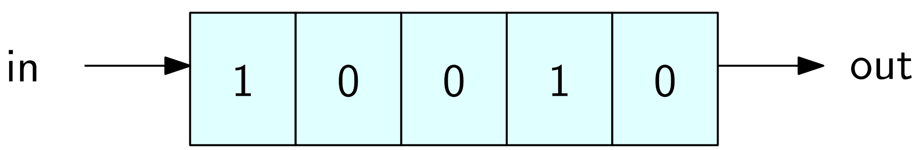
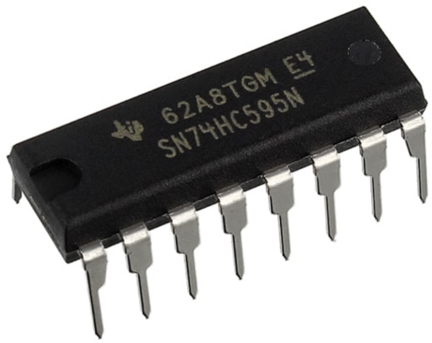
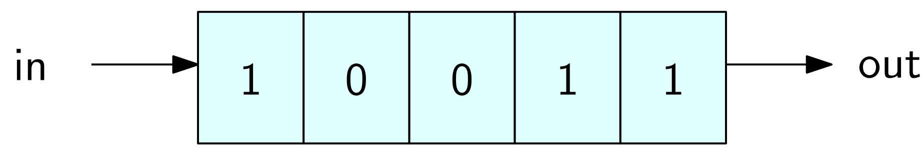
We use a simplified graphical depiction:





Linear Feedback Shift Registers (LFSR)

The value of the “in” line is the XOR of a subset of the bits in the register



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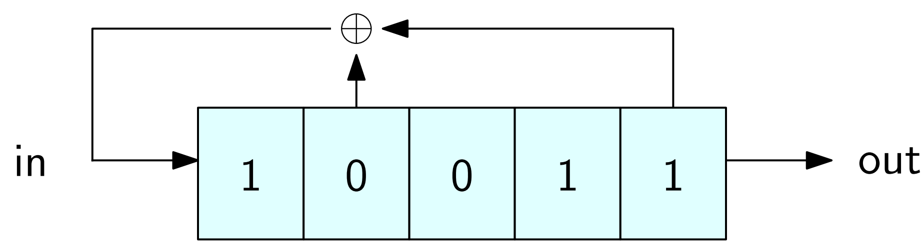

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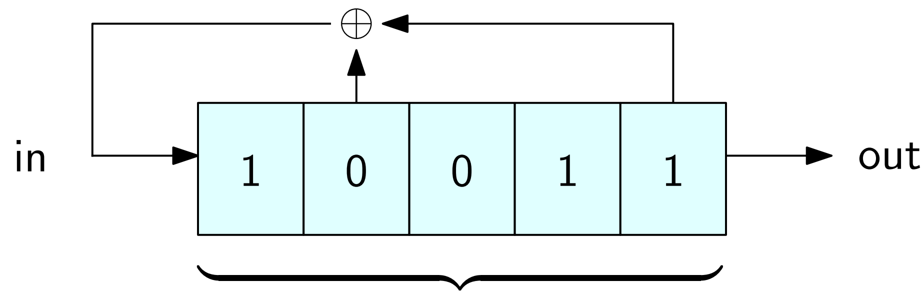

the number of bits is called
the **degree** of the FSR

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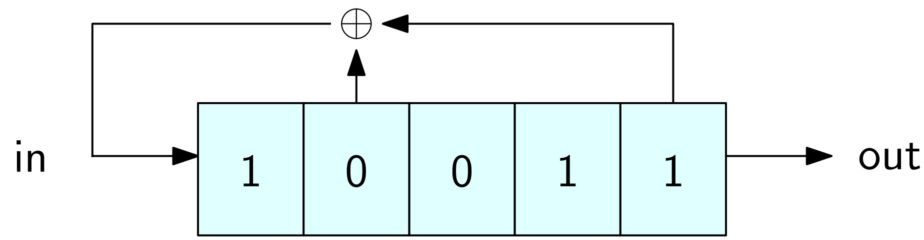

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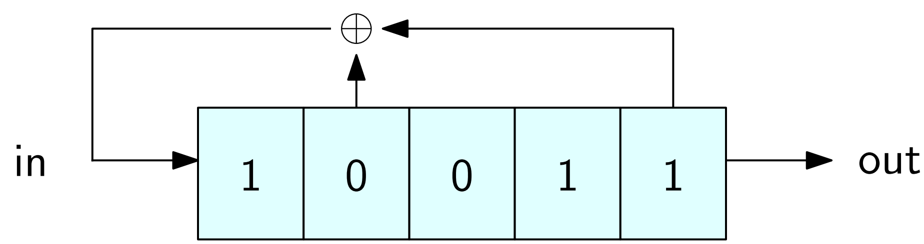

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At each clock tick:

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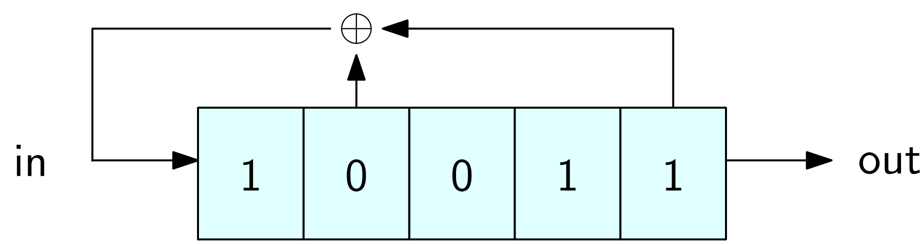

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Sequence of states and output bits in the above example:

- States: 10011
- Outputs:

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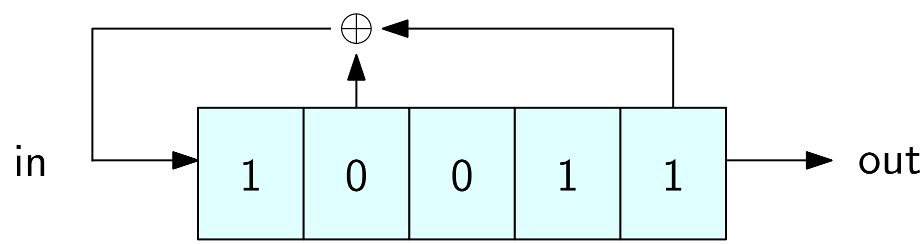

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Sequence of states and output bits in the above example:

- States: 10011 $\rightarrow$ 11001
- Outputs: 1

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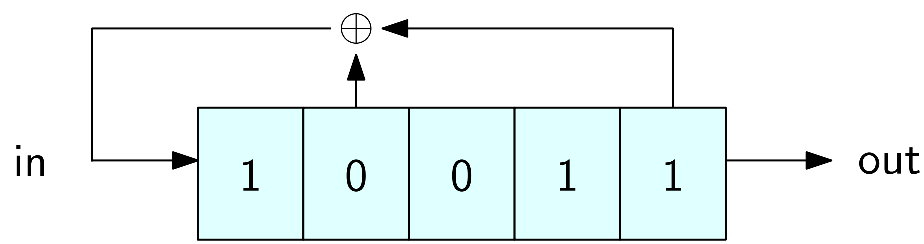

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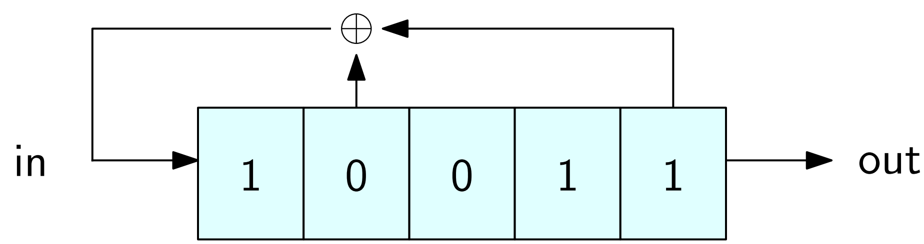

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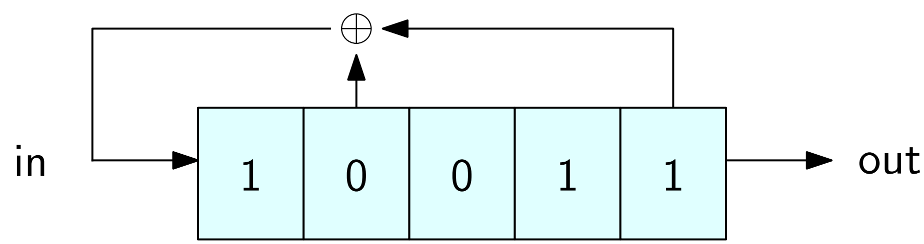

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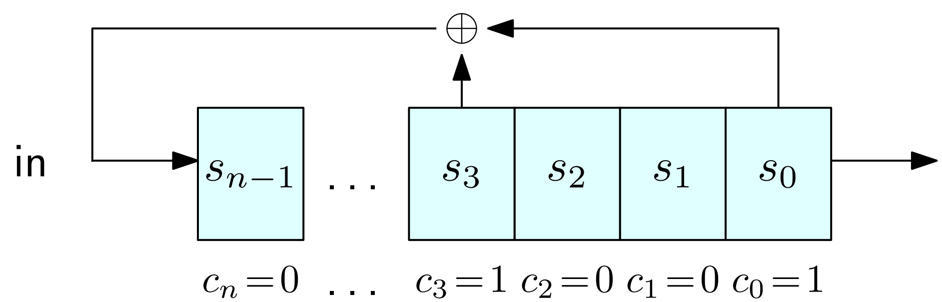
- Outputs: $1 \quad 1 \quad 0 \quad 0$

Linear Feedback Shift Registers (LFSR)

The subset of bits that are XOR-ed together can be described by n coefficients $c_0, c_1, \ldots, c_{n-1}$



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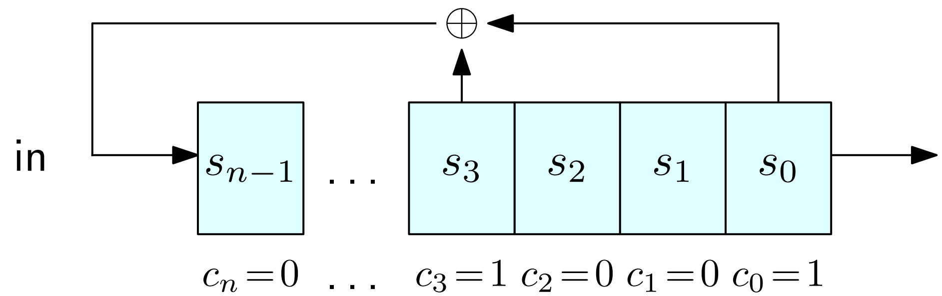

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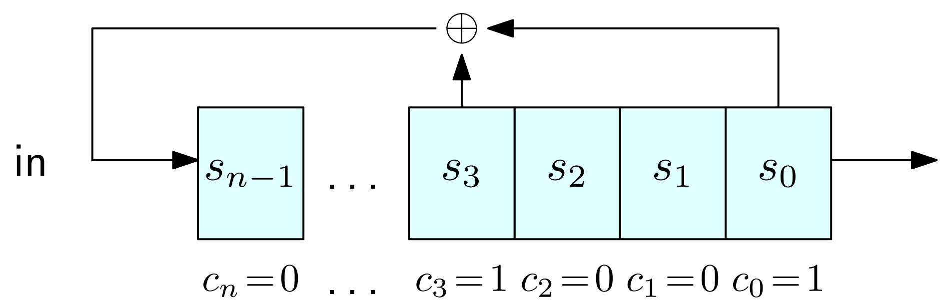

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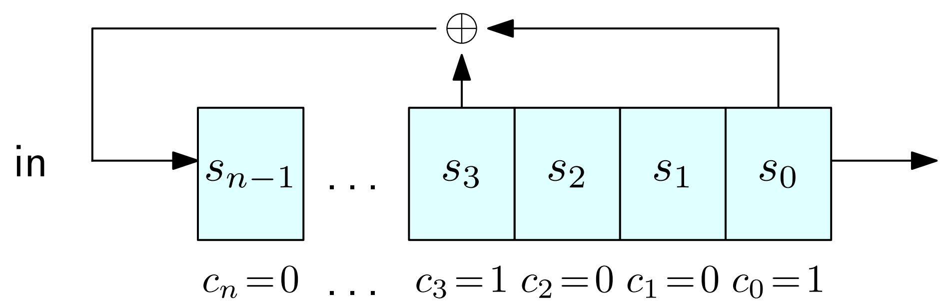

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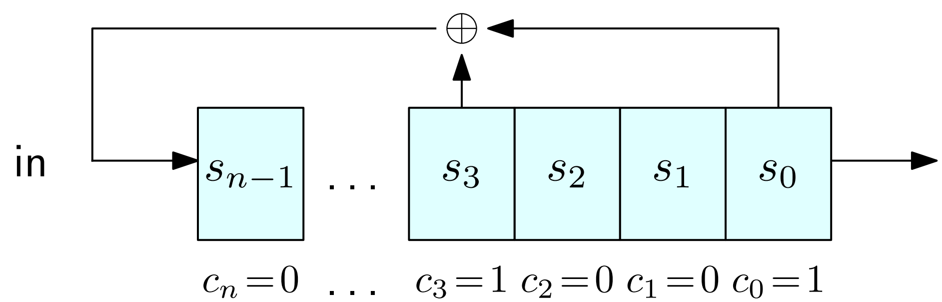

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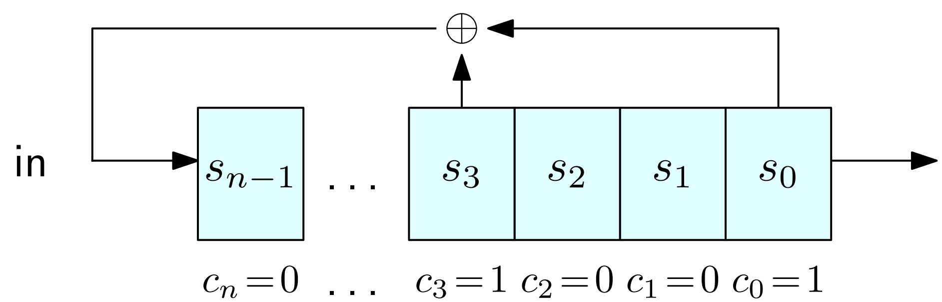

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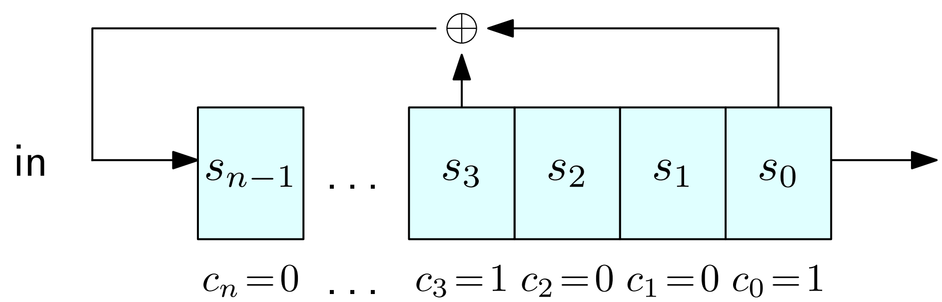

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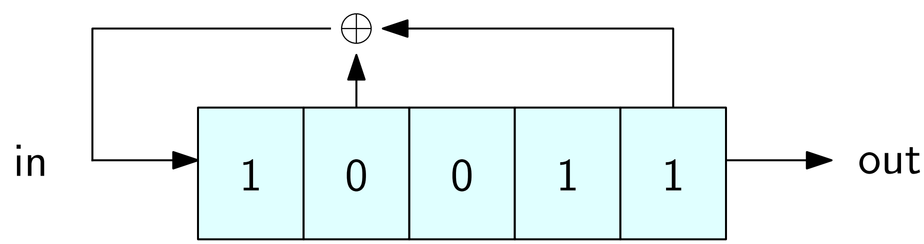
The coefficients are part of the construction of the LFSR.

By Kerckhoffs' principle they should not be considered secret

LFSRs as stream ciphers



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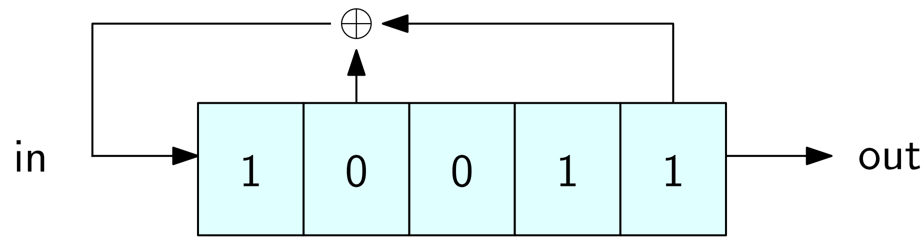

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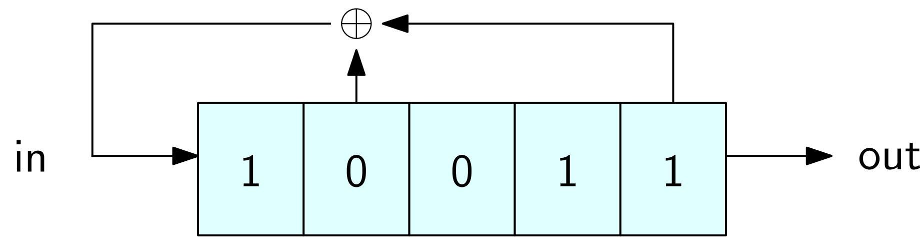

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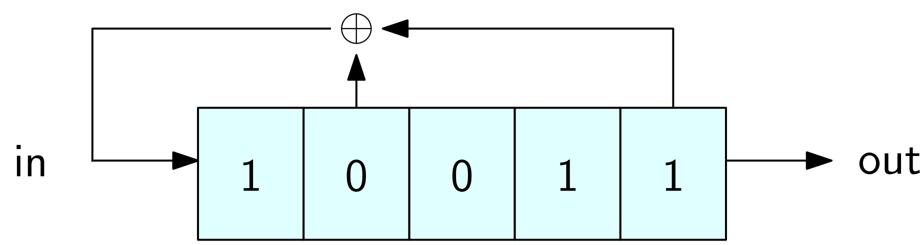

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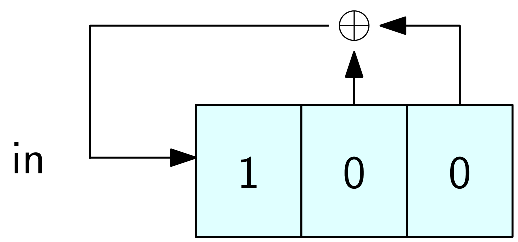
A necessary (but not sufficient) condition for stream ciphers to be secure is that the time it takes for repeats to happen must be long

State Graph

Given a FSR



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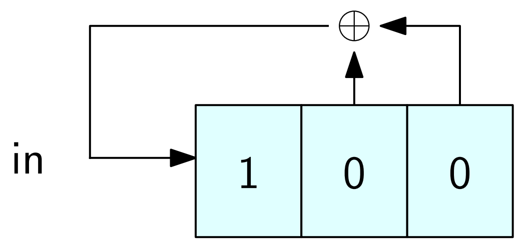

We can create a **state graph** $G = (V, E)$ in which each vertex is a state, i.e., $V = \{0, 1\}^n \ldots$

$\ldots$ and there is a directed edge labelled $y \in \{0, 1\}$ from st to st$'$ iff Next(sf) $= (y, \mathsf{sf}')$.

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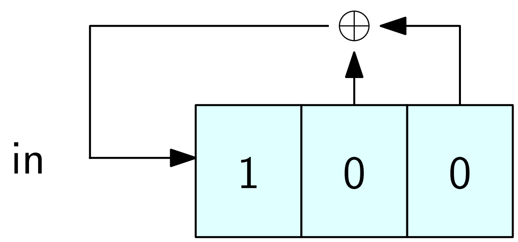

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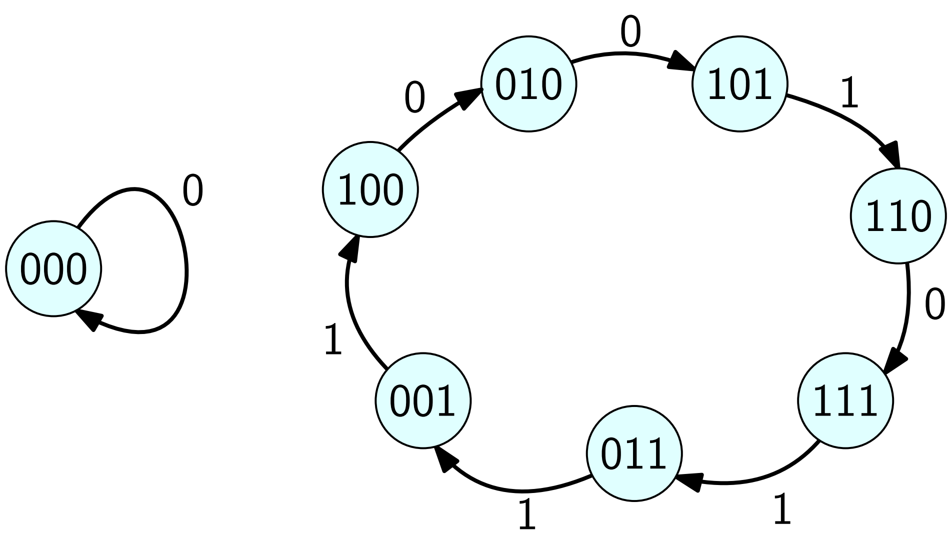

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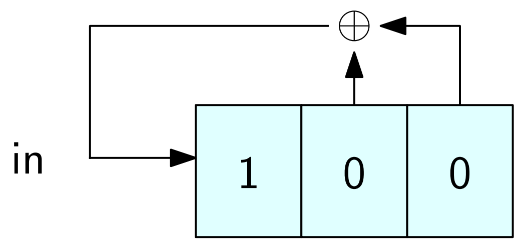

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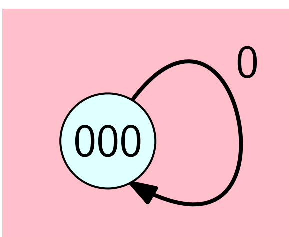

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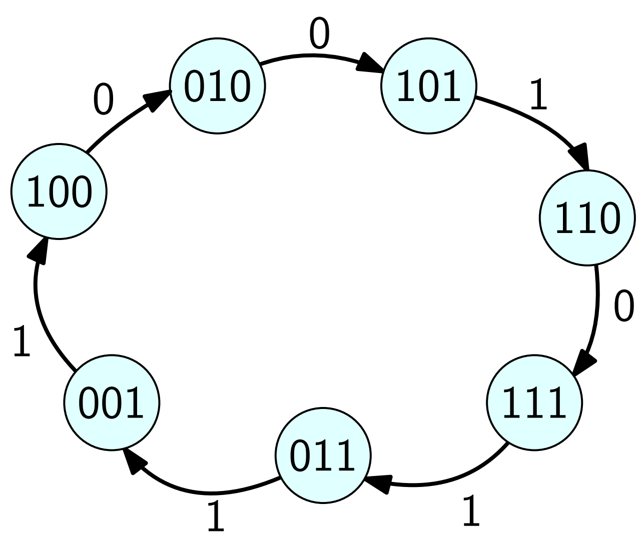
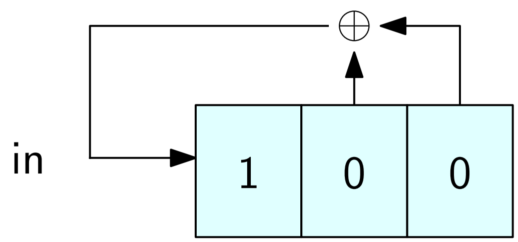


State Graph

Given a FSR



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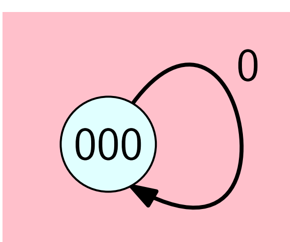

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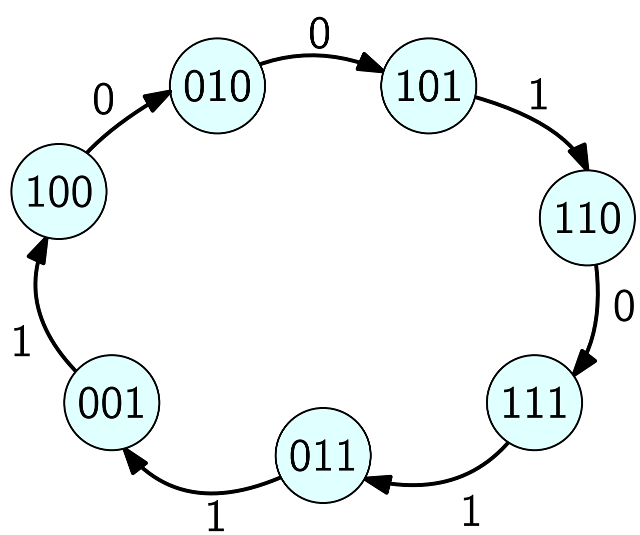

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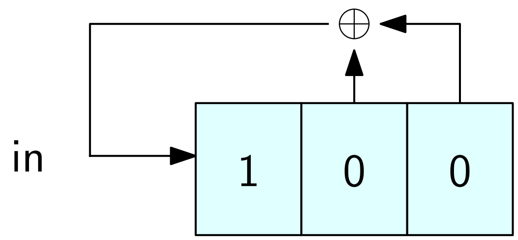

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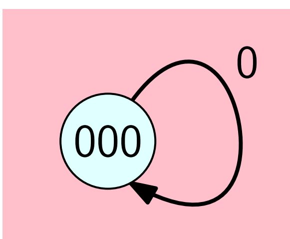

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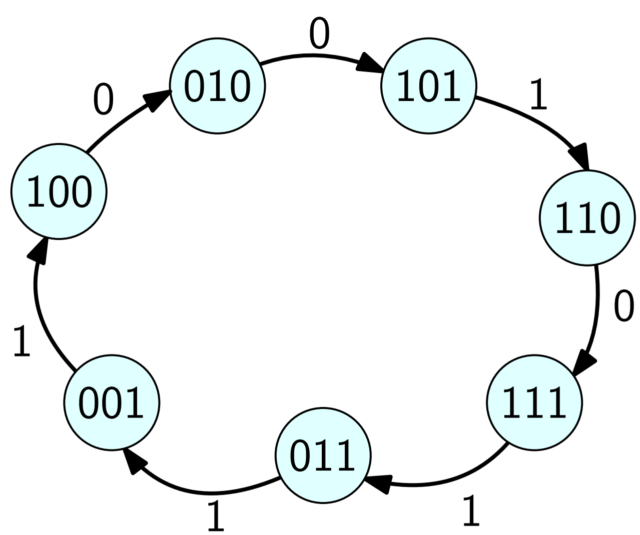

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For any n, it is known how to set the coefficients to obtain a maximum length LFSR of degree n

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- n variables
- If the LFSR has maximum length*, then the equations are linearly independent

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$\Downarrow$

Unique solution! Solve the system and recover all coefficients

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The output of a maximum-length LFSR of degree 4 is:

$$\begin{array}{c} y_0 y_1 y_2 y_3 y_4 y_5 y_6 y_7 \\ 0, 0, 1, 1, 1, 1, 0, 1 \end{array}$$

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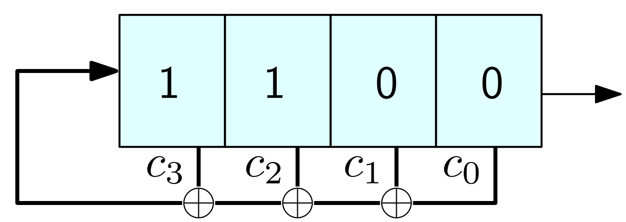

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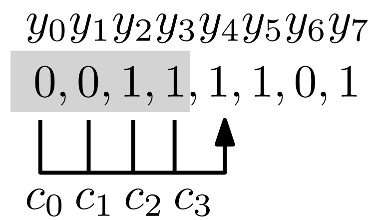

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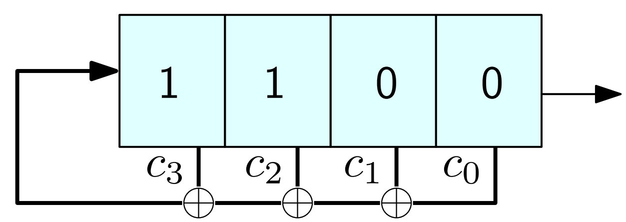

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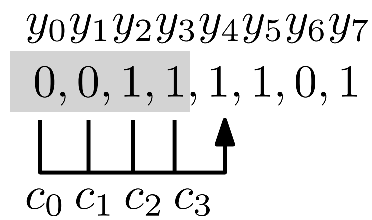

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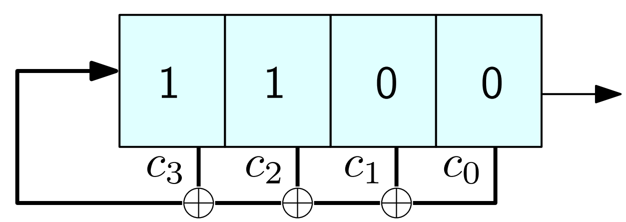

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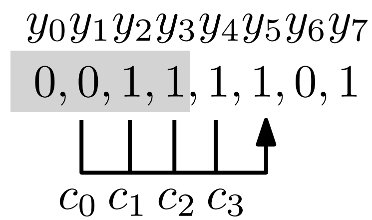

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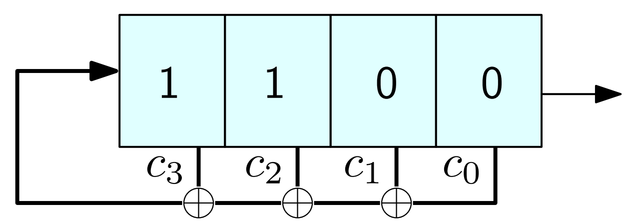

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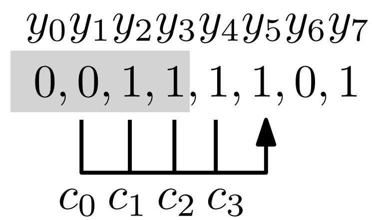

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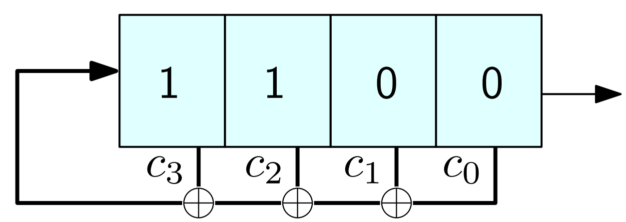

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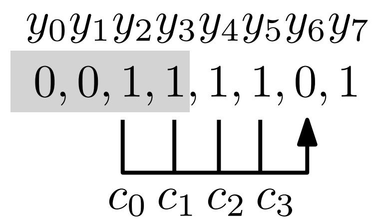

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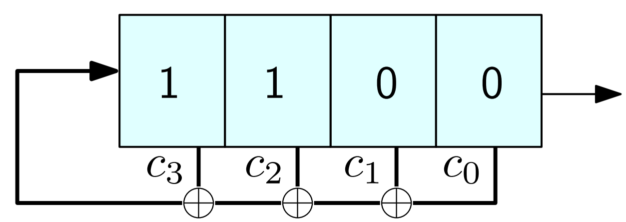

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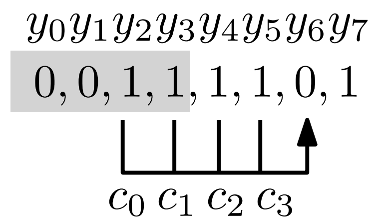

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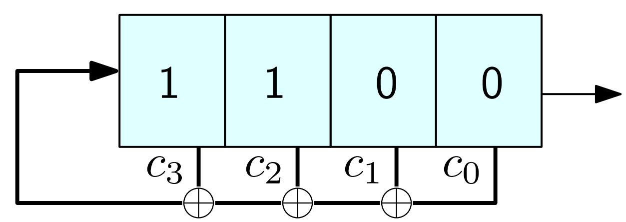

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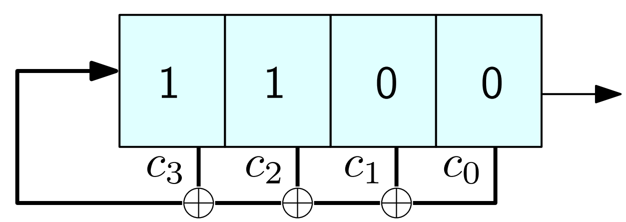

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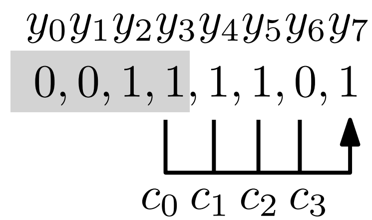

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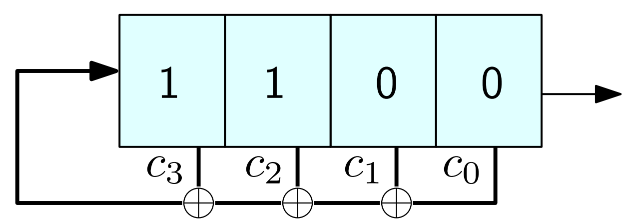

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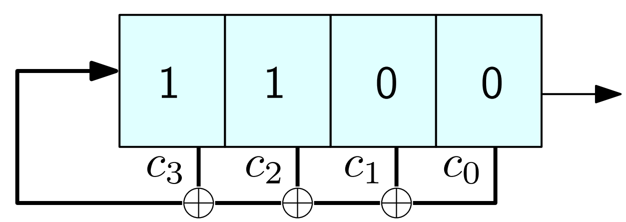

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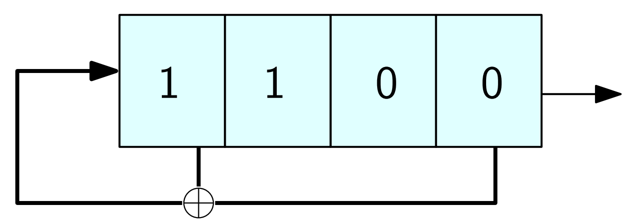

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- **Combination generators:** use multiple LFSRs and combine their outputs in some nonlinear way

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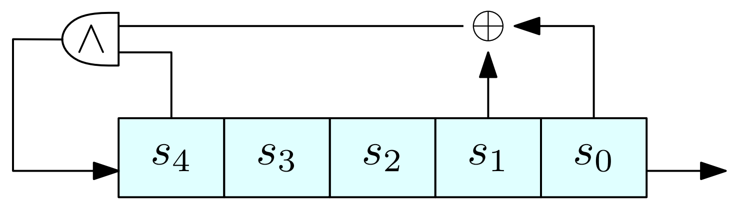

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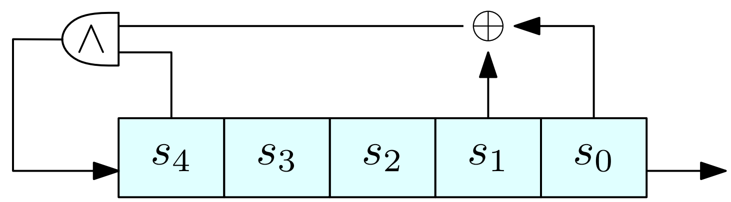

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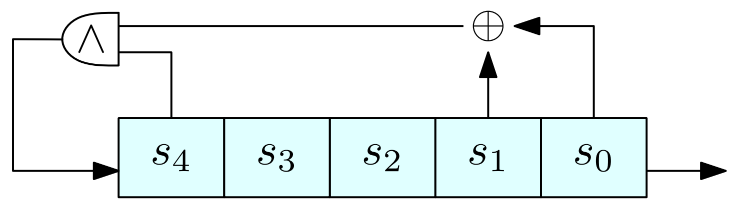

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  The function g above is not a great choice, since its is 0 whenever at least one of $s_0 \oplus s_1$ and s_4 is 0

  If we heuristically think of the state as a uniformly random string, then $g(\cdot)$ will be zero 75% of the time!

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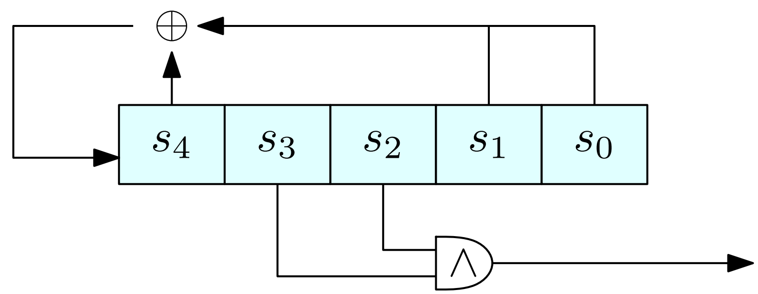

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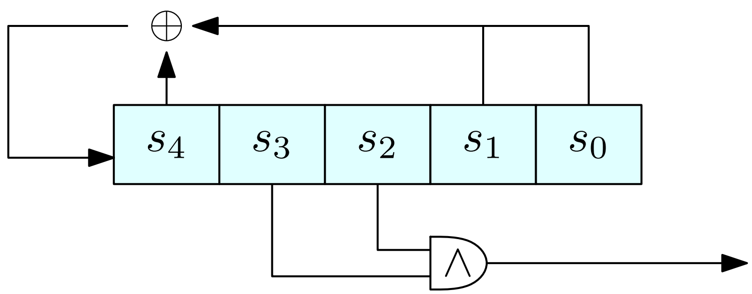

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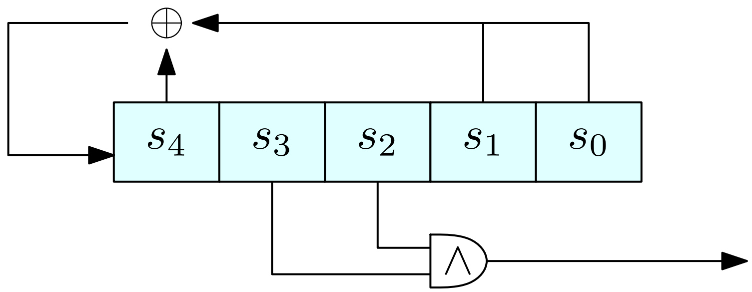

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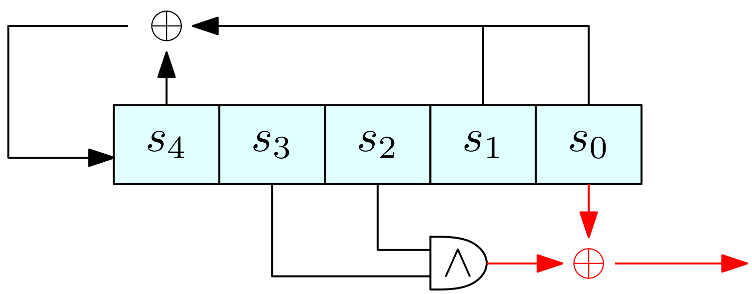

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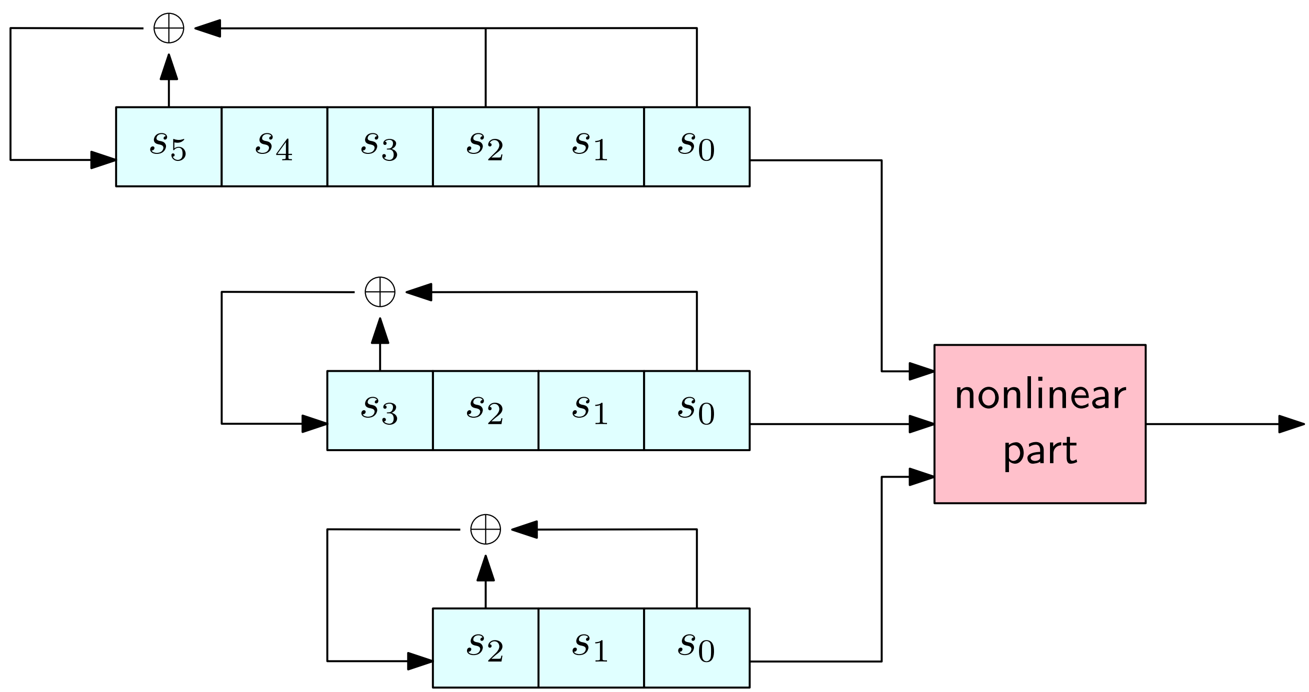
- The function $g(\cdot)$ is called **filter**
- Care must be taken to ensure that $g(\cdot) = 1$ with probability $\approx \frac{1}{2}$
- A better function: $g(s_0, s_1, \ldots, s_{n-1}) = (s_2 \wedge s_3) \oplus s_0$

Adding nonlinearity

Combination generators: use multiple LFSRs and combine their outputs in some nonlinear way



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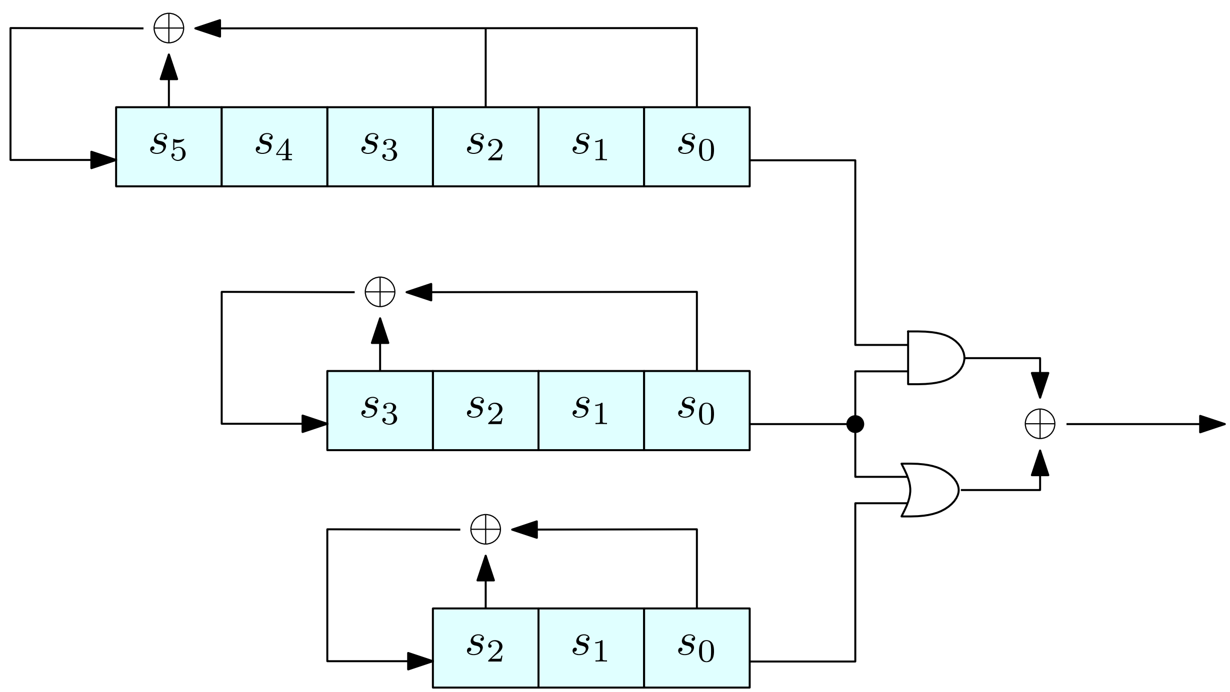

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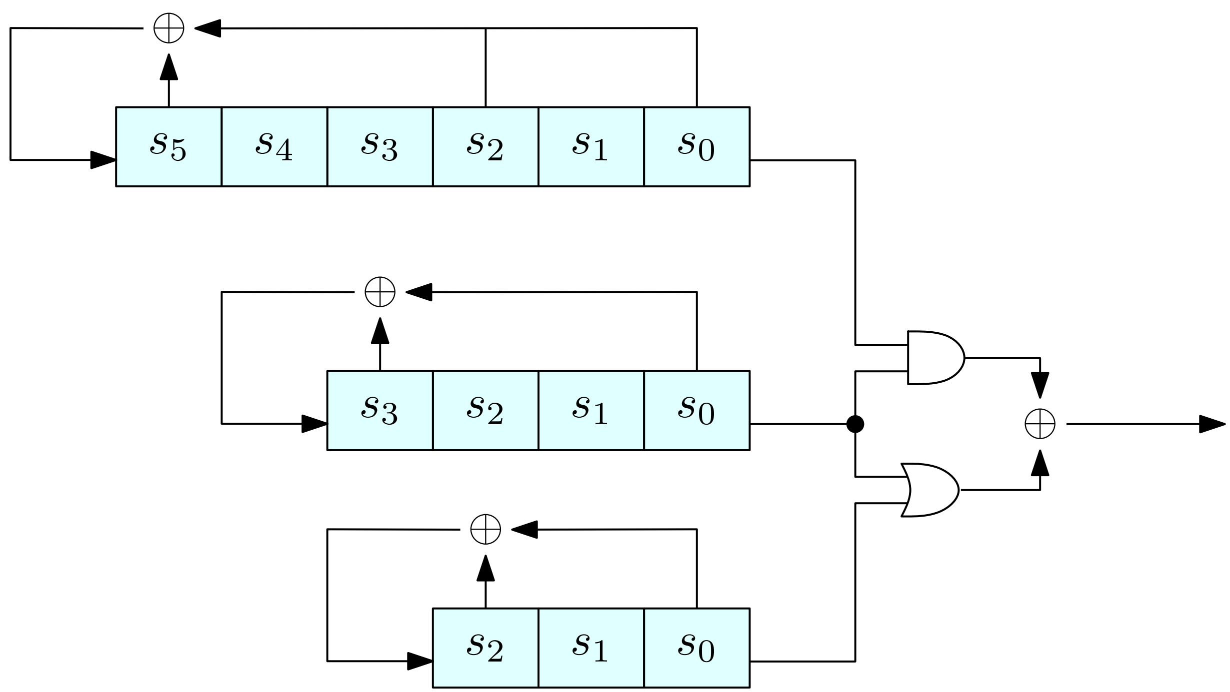

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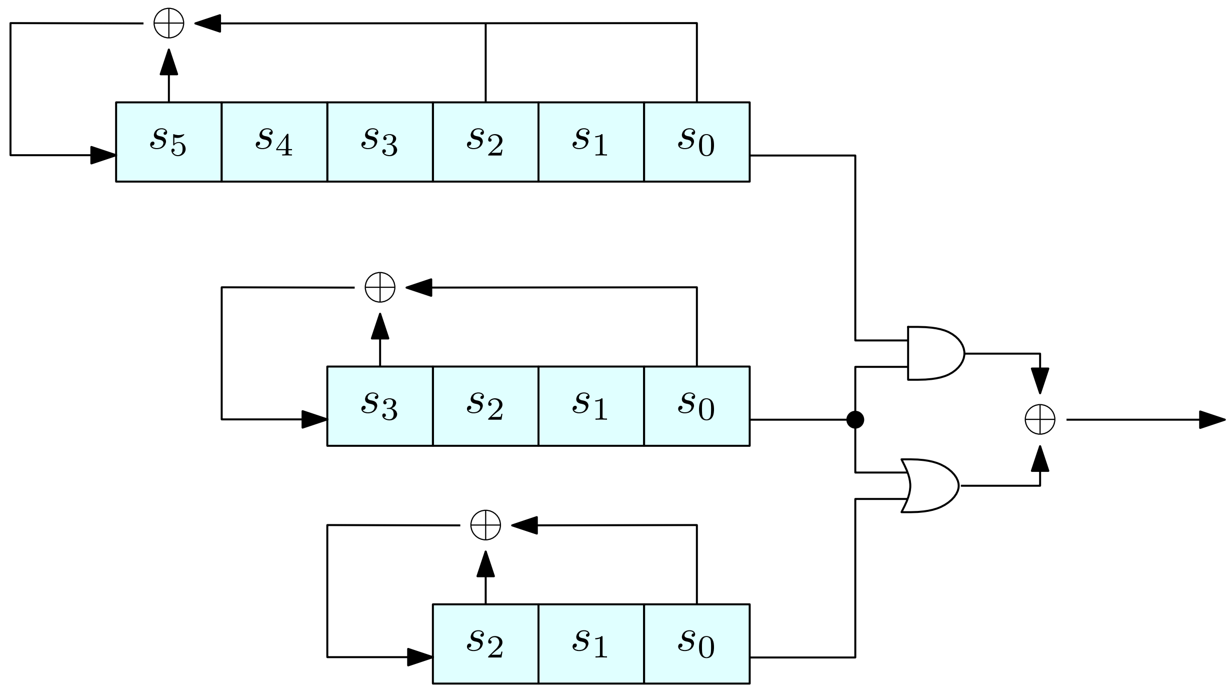
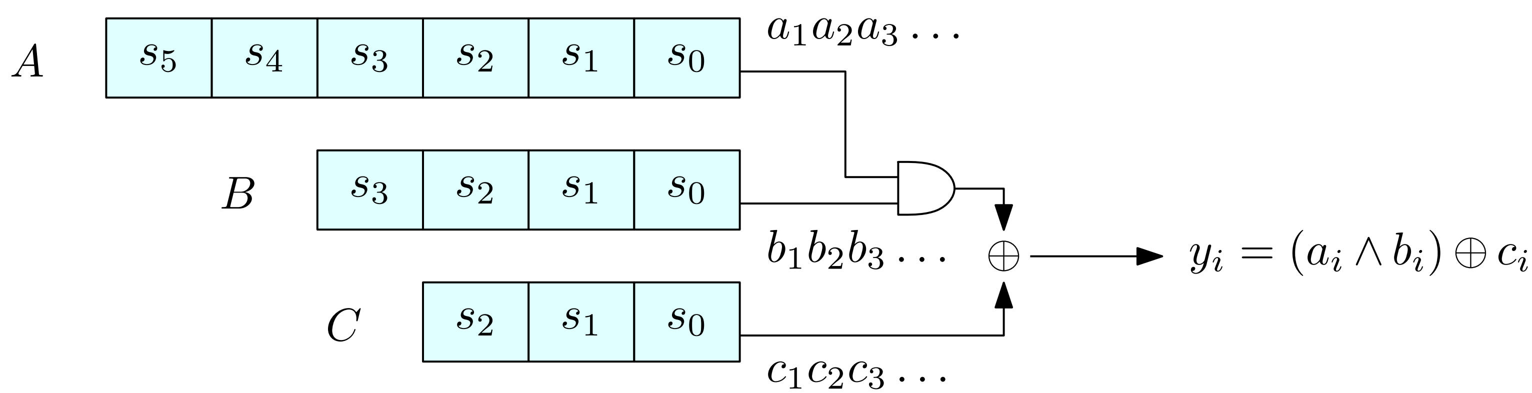


- The LFSRs do not need to have the same degrees (in fact, it is better if they have different degrees)
- Ideally, if the degrees are $d_1, d_2, d_3, \ldots$, we would like attacks to take time $\approx 2^{d_1+d_2+d_3+\cdots}$

Correlation attacks on combination generators

Care must be taken to ensure that the output bit is not biased towards the output of any of the LFSRs

A bad example:



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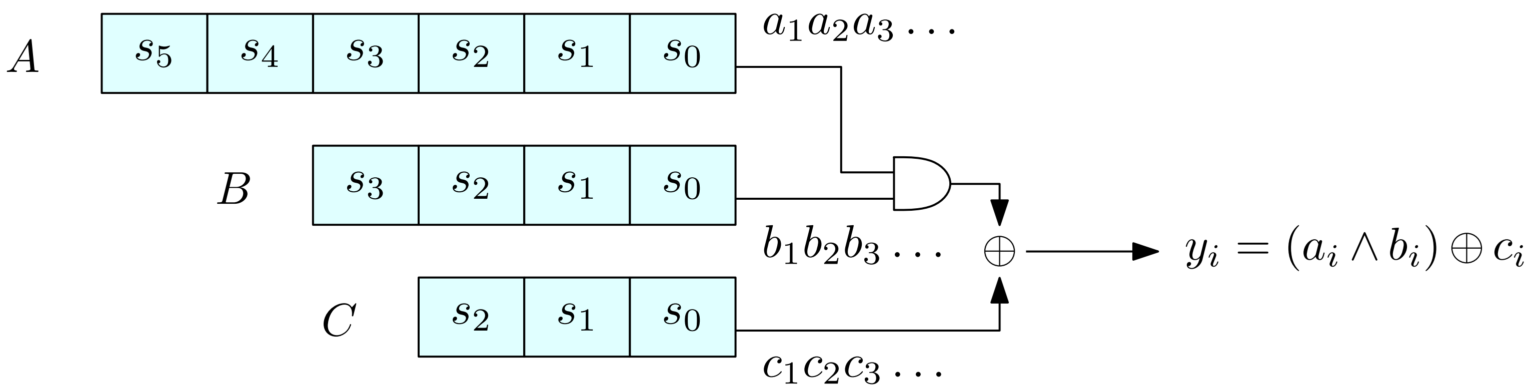

- 75% of the time $(a_i \wedge b_i)$ is 0
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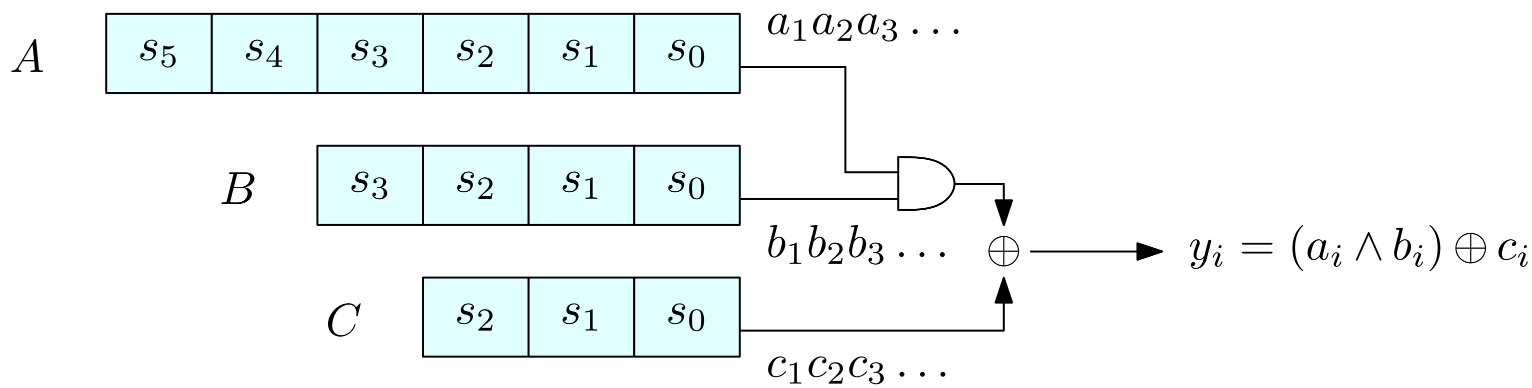
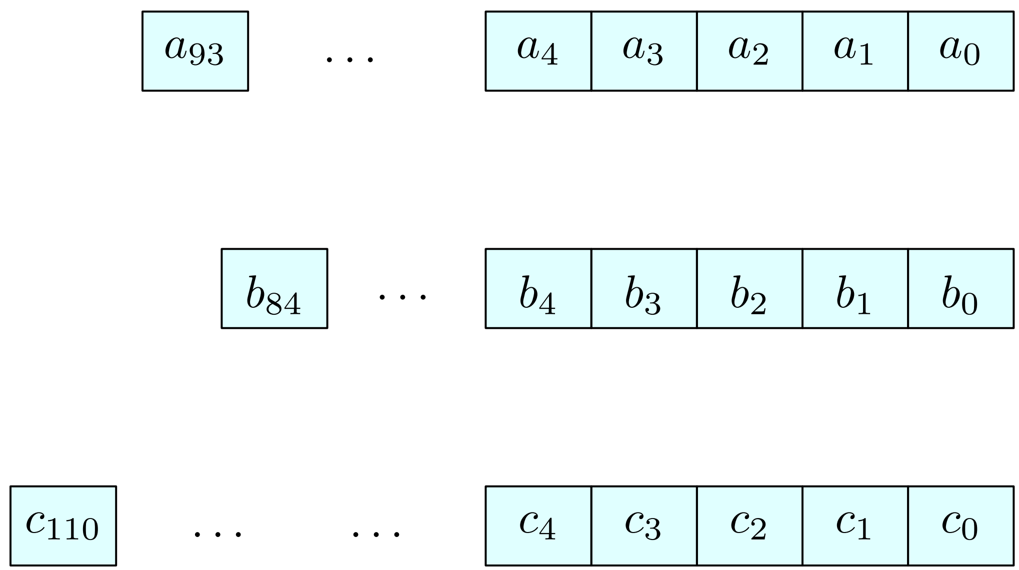


- 75% of the time $(a_i \wedge b_i)$ is 0
- When this happens, $y_i = c_i$
- We can run a bruteforce attack on C:
  - Try all possible initial states. For every state generate a stream of bits $c'_1, c'_2, c'_3, \dots$
  - When the initial state is correct, $\approx 3/4$ of the bits c_is match with the corresponding c'_is

Back to Trivium

- Three FSRs (say A, B, C) of degrees 93, 84, and 111 (overall, the state is 288 bits long)



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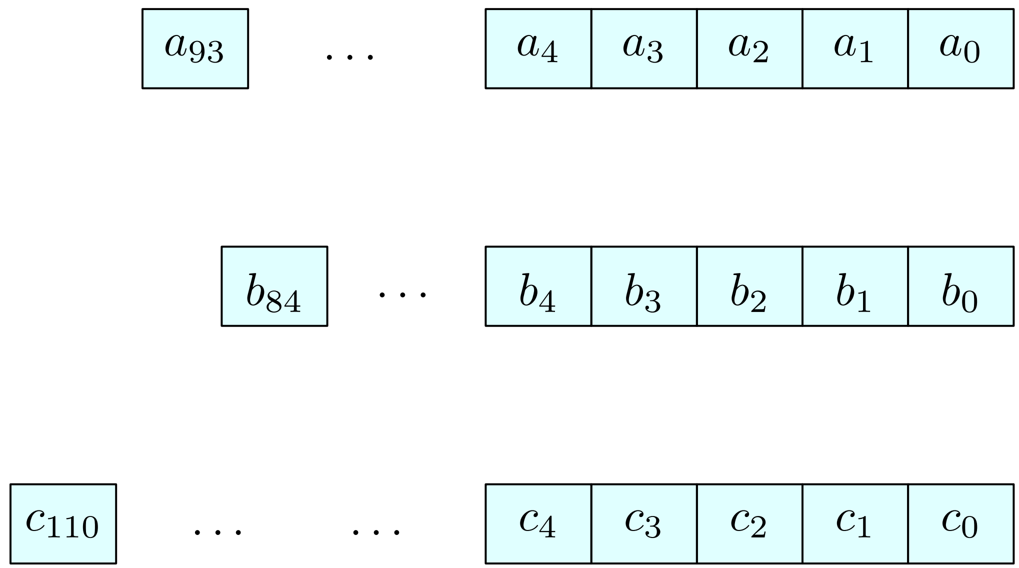

- The FSRs are **coupled**: the input of each FSR is a non-linear function of a register from that FSR, and of 4 registers from another FSR

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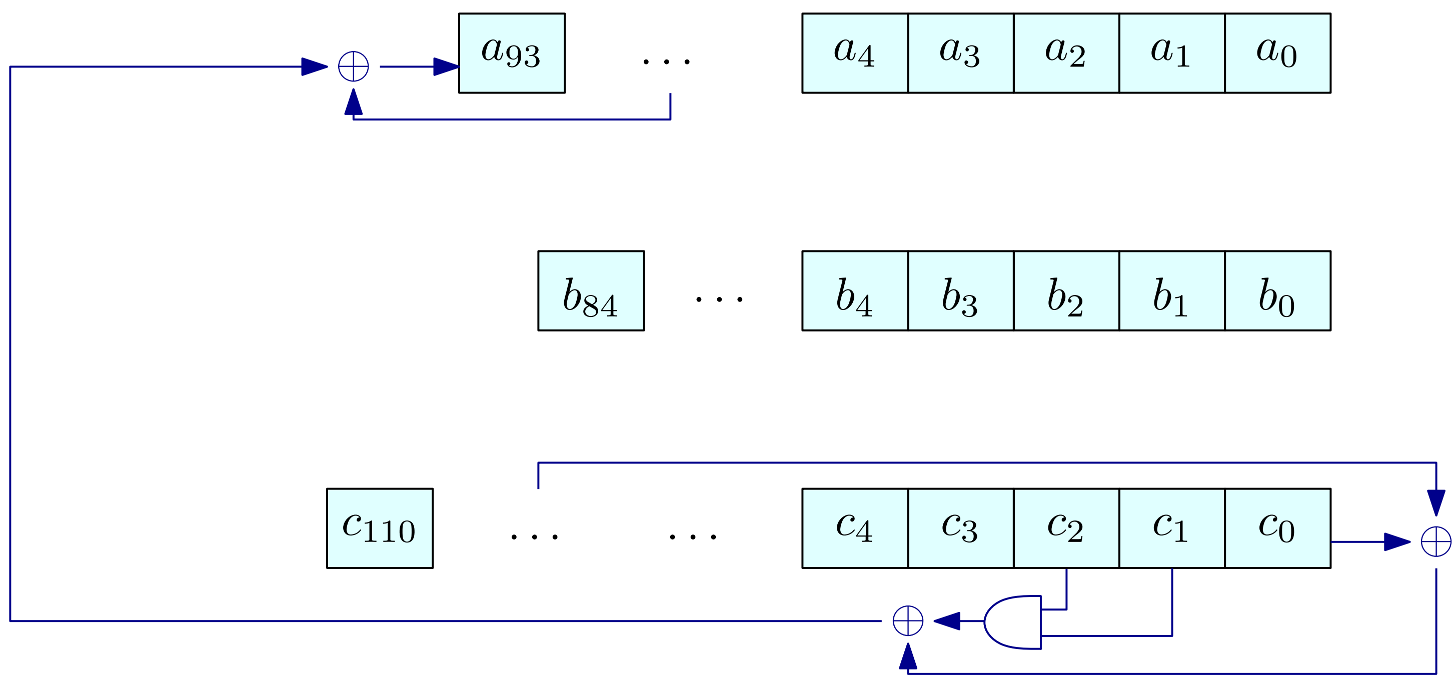

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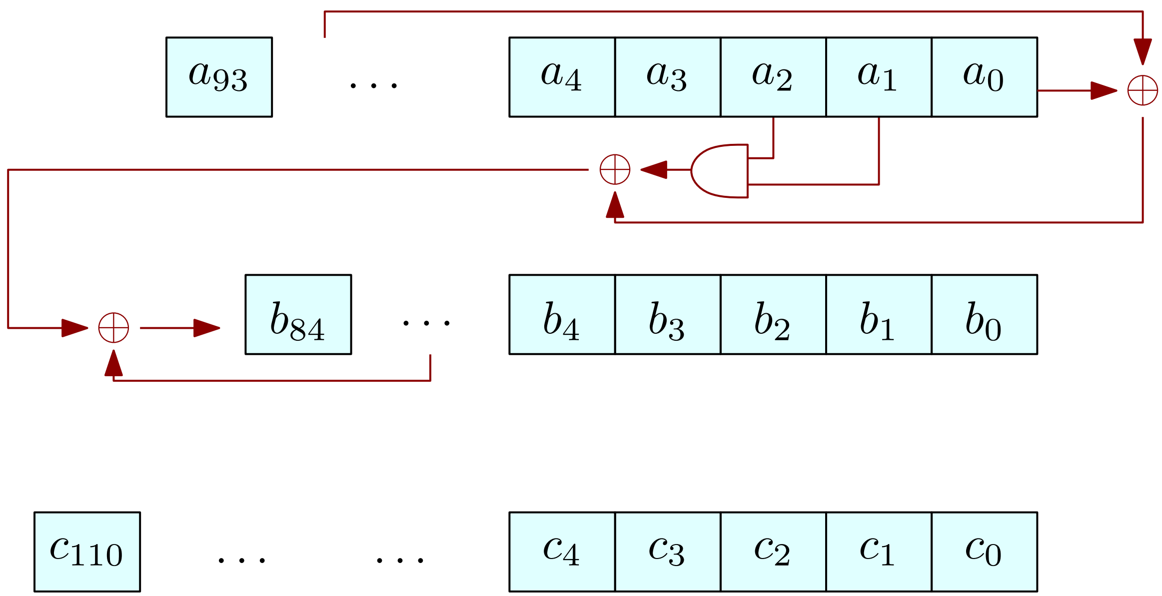

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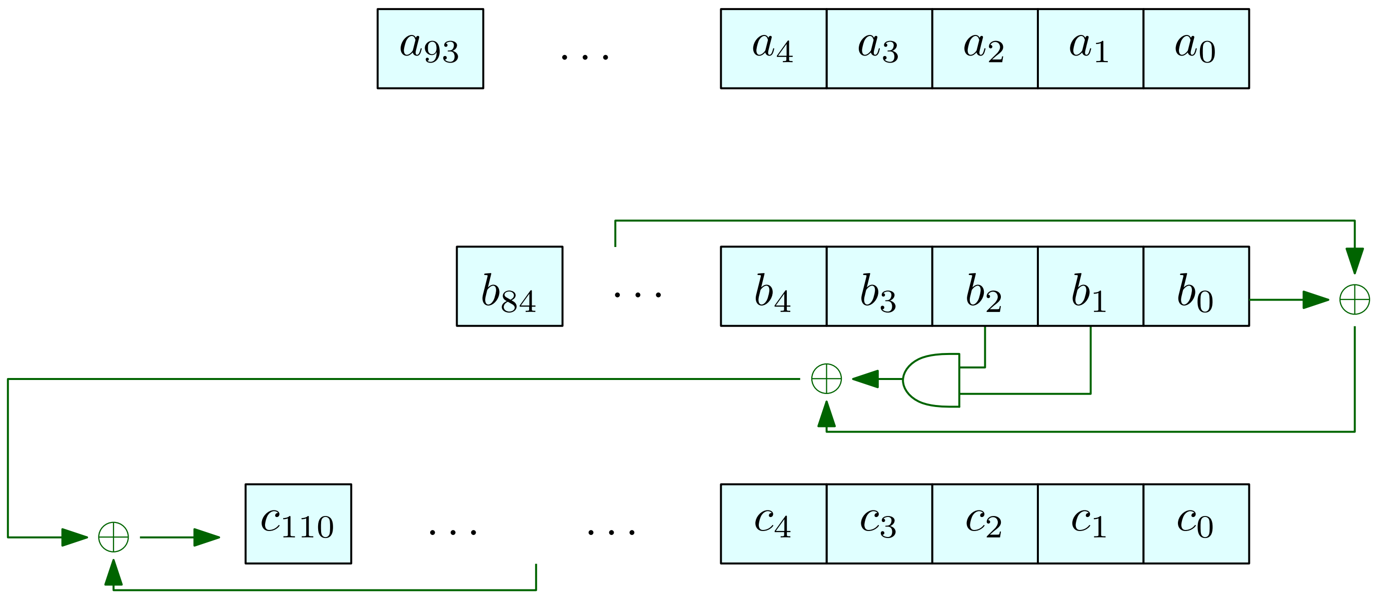

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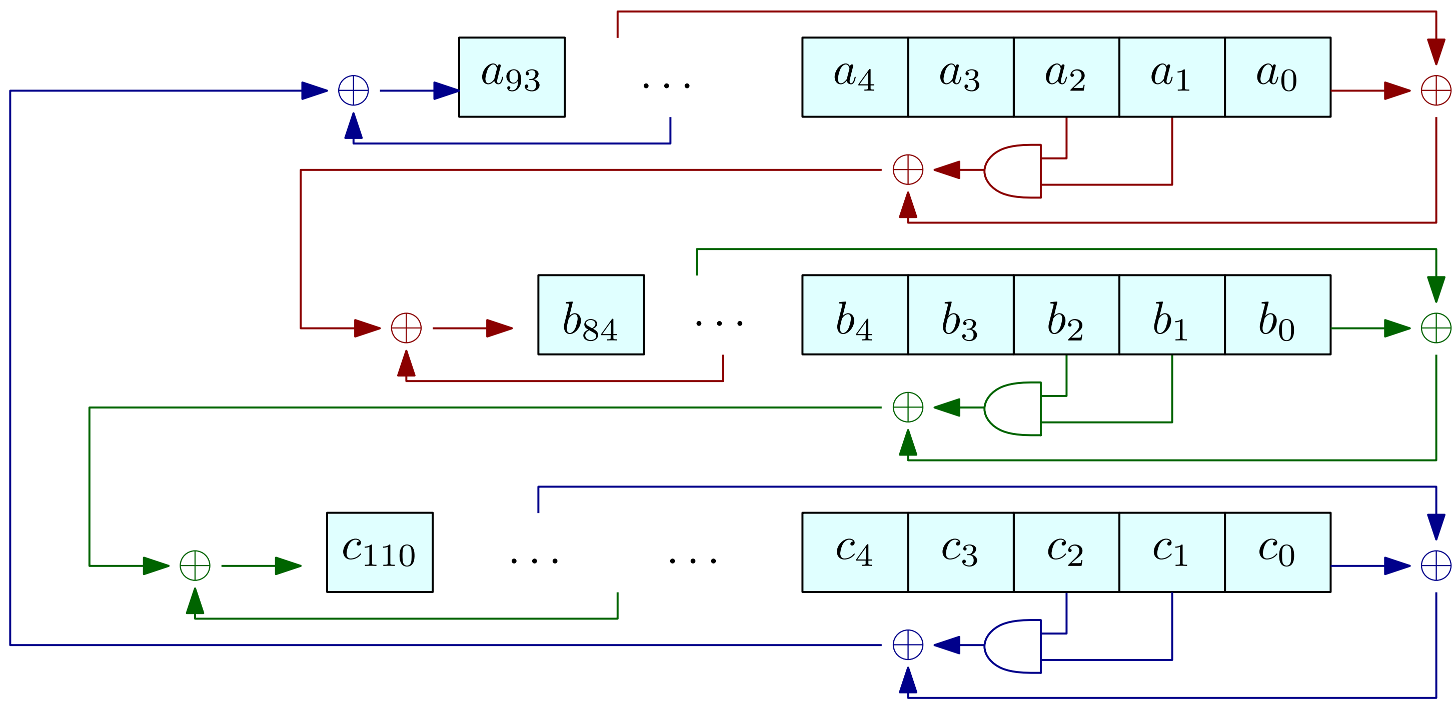

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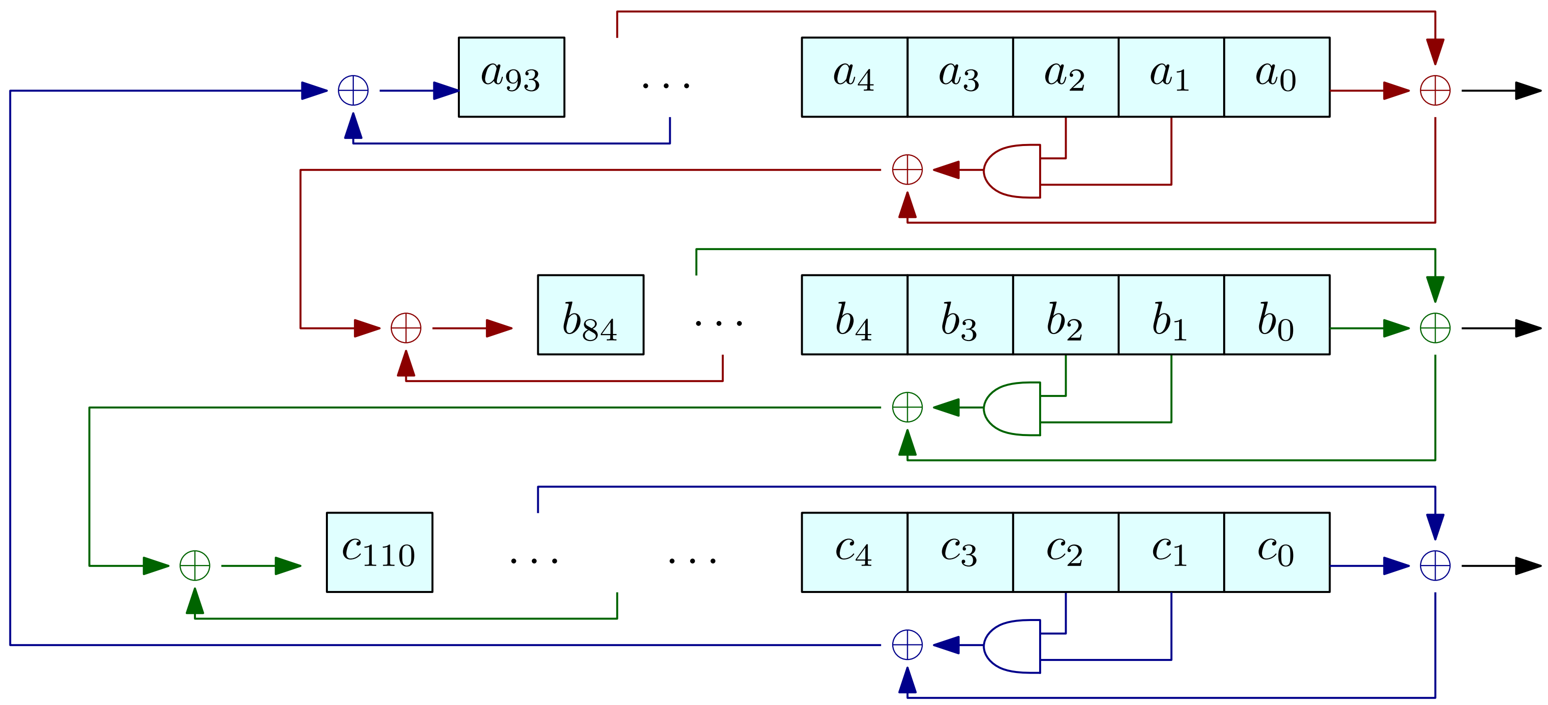

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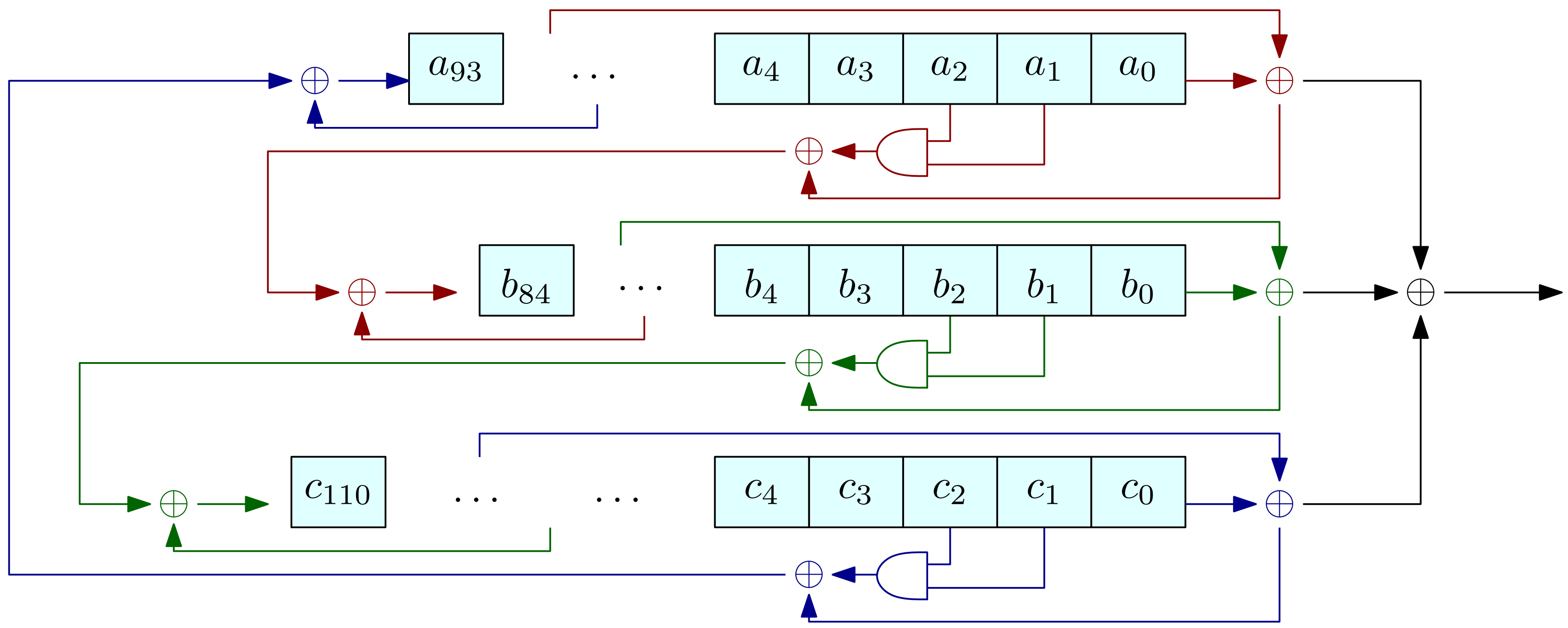


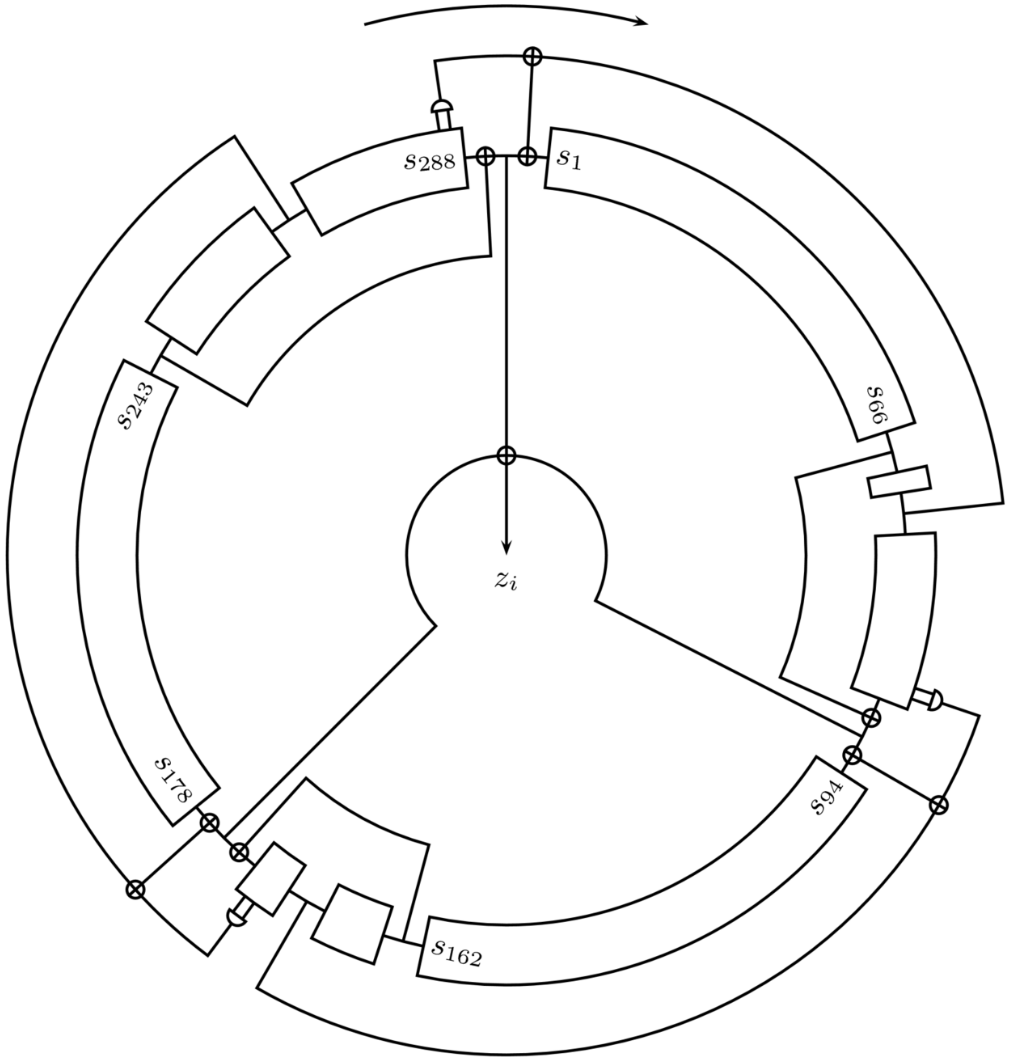
- The output of each FSR is the XOR of its rightmost bit plus the content of another register
- The output of Trivium is the XOR of the outputs of the single FSRs

Trivium: Init

Trivium takes a 80-bit key and a 80-bit IV... and generates up to 2^{64} bits of output

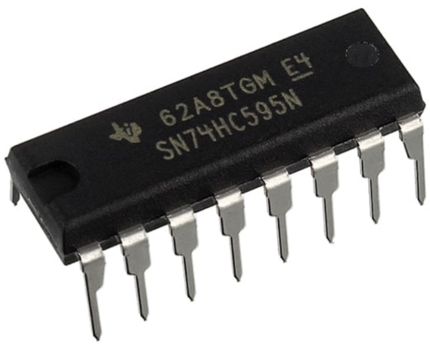
Init:

- Set the leftmost 80 registers of A to the key, and other registers to 0
- Set the leftmost 80 registers of B to the IV, and other registers to 0
- Set the rightmost 3 registers of C to 1, and other registers to 0
- Run for $4 \cdot 288$ clock ticks and discard the output


s_{288}
s_1
s_{99}
s_{243}
z_i
s_{178}
s_{94}
s_{162}

Extra: Implementing LFSRs in hardware

8 bit shift register



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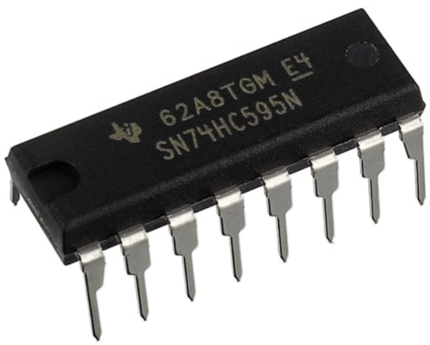

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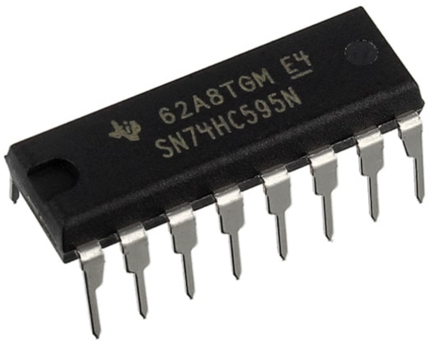

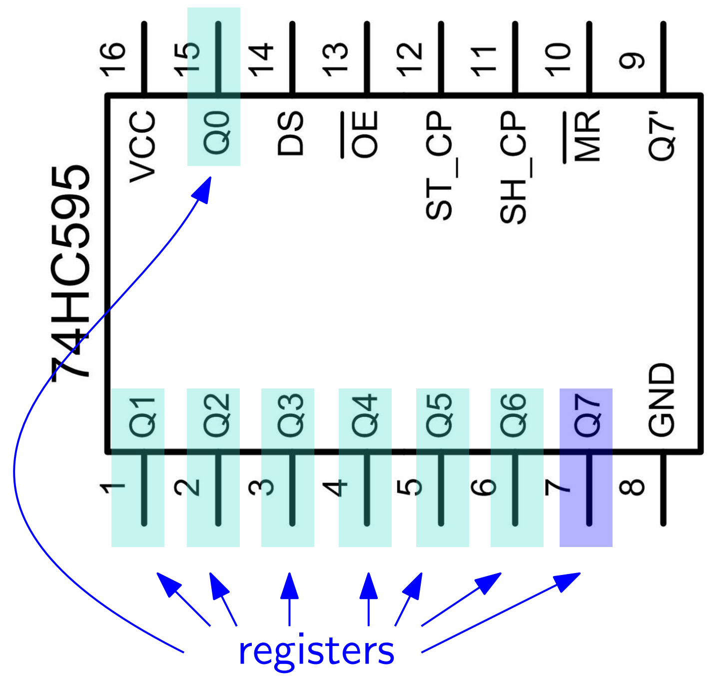

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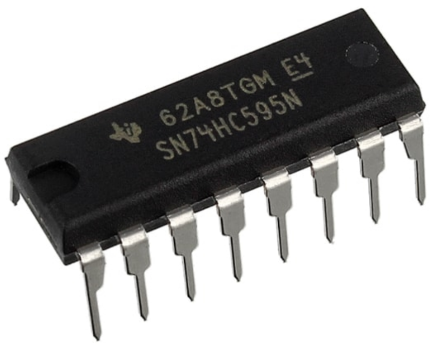

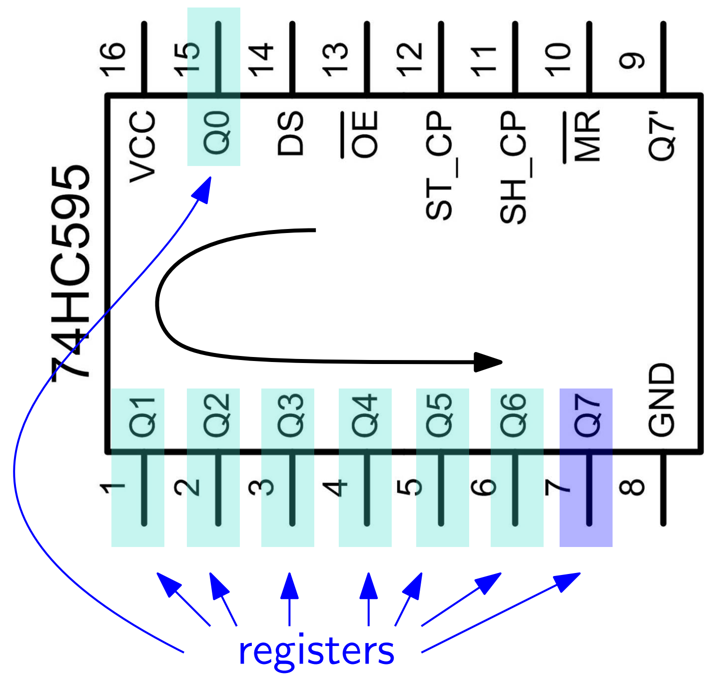

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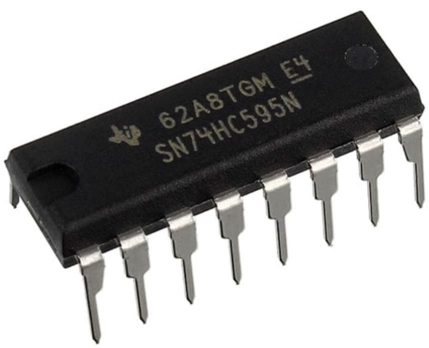

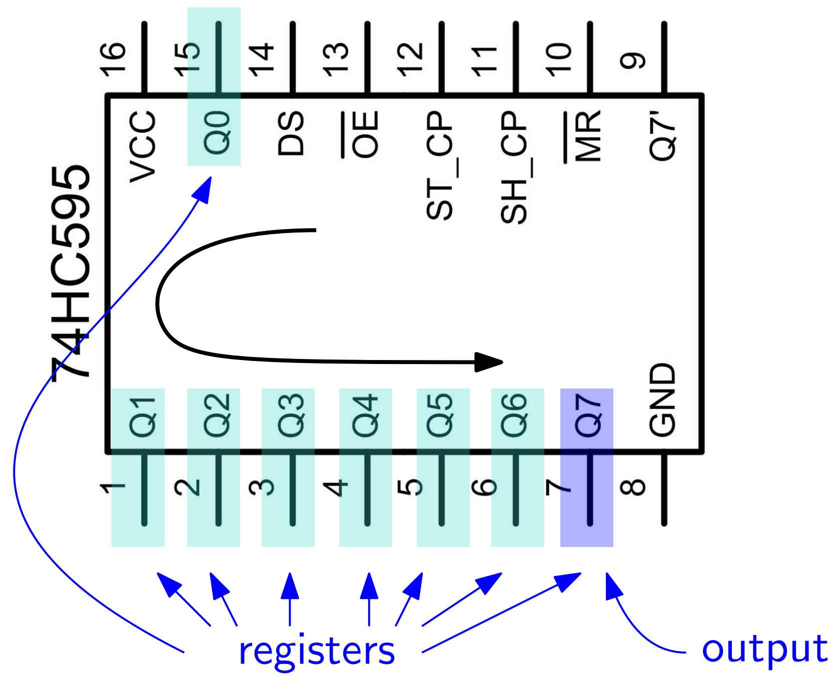

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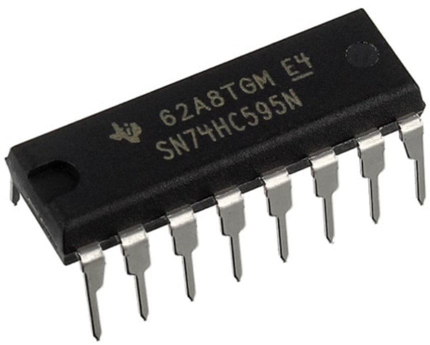

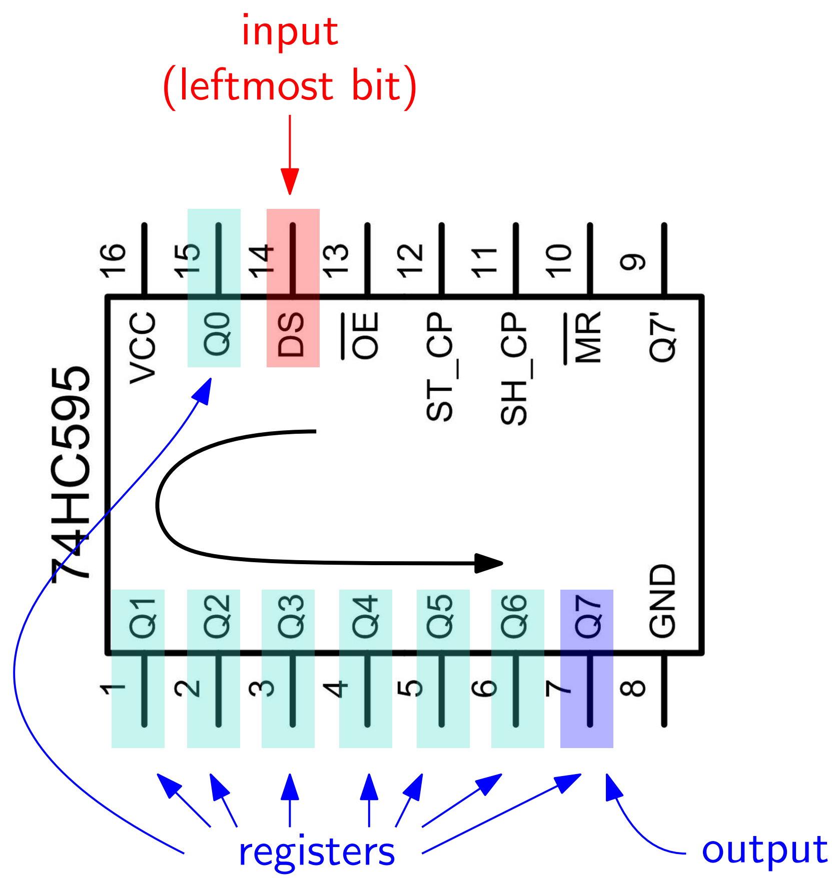

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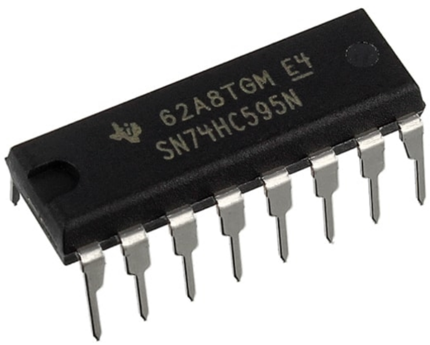

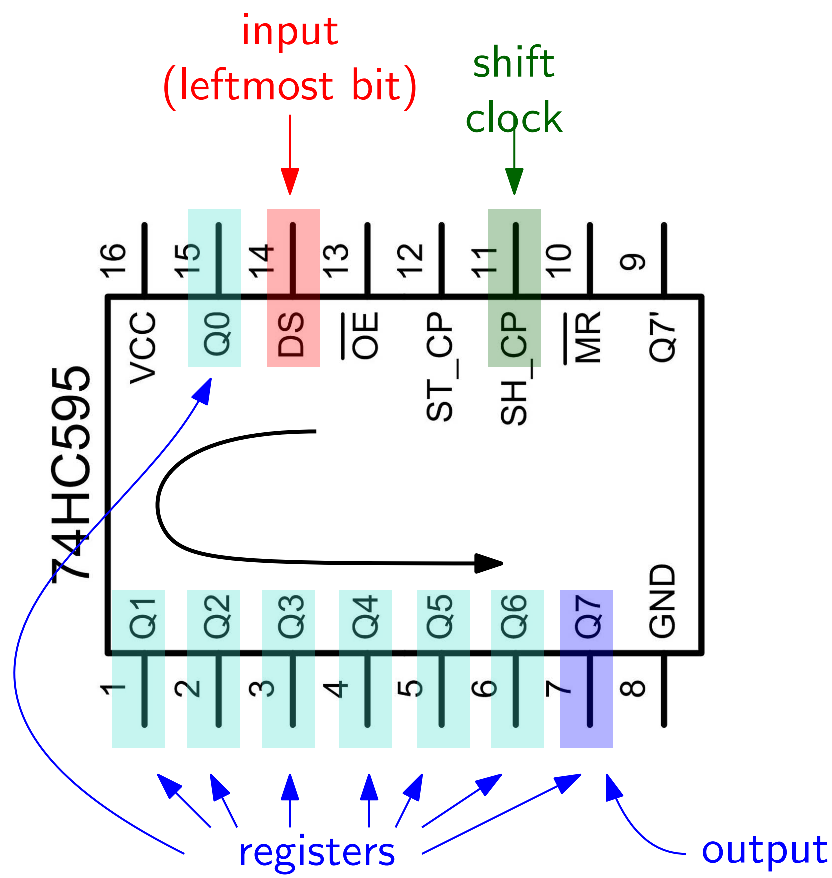

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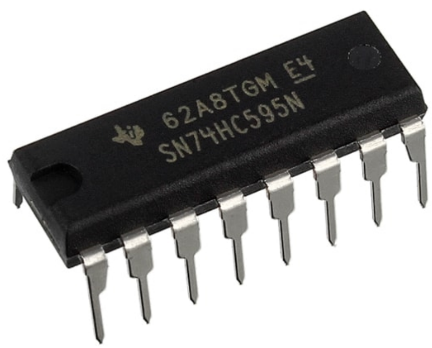
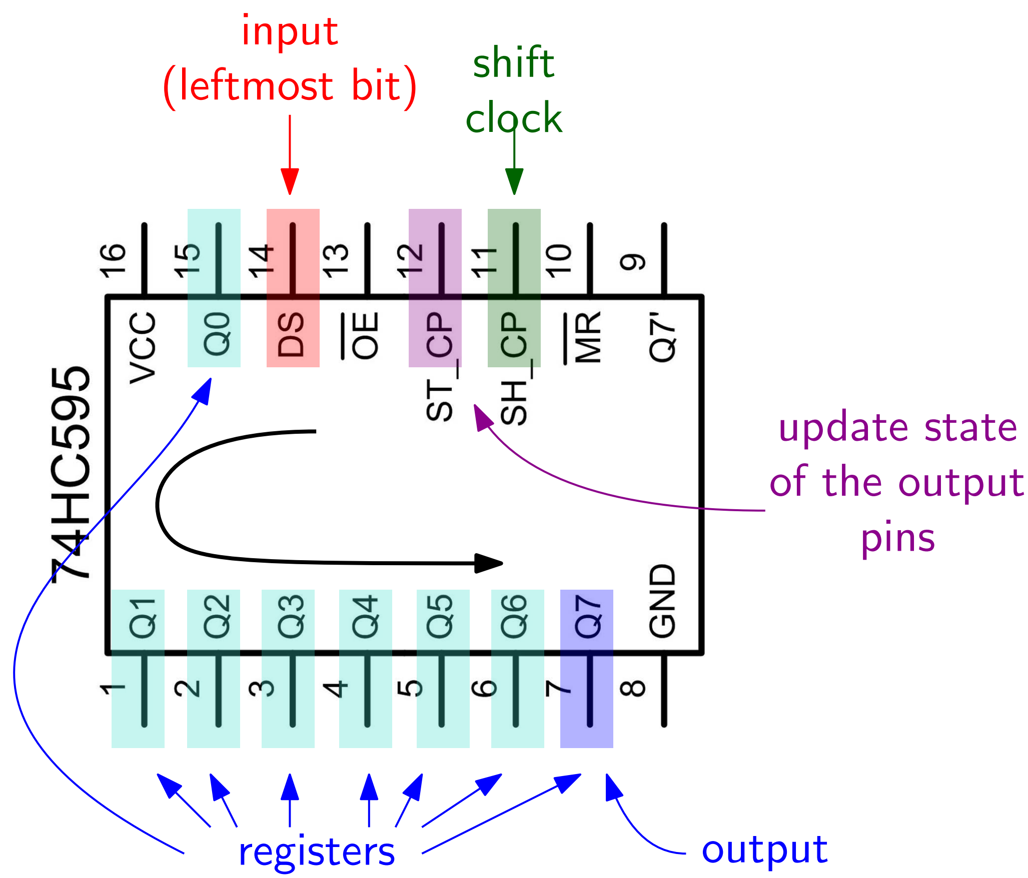
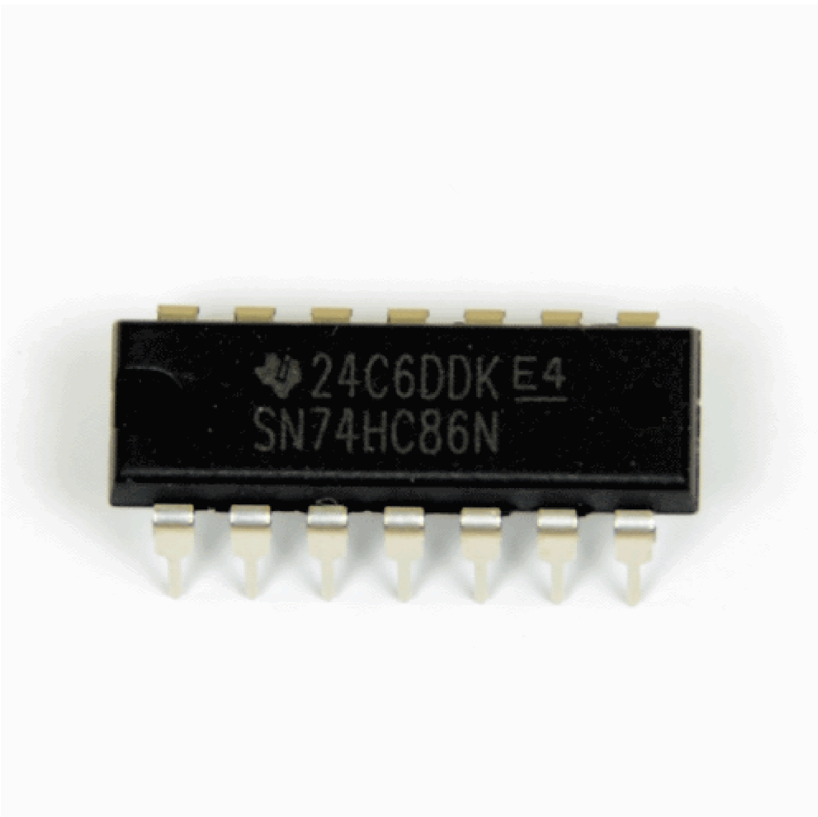
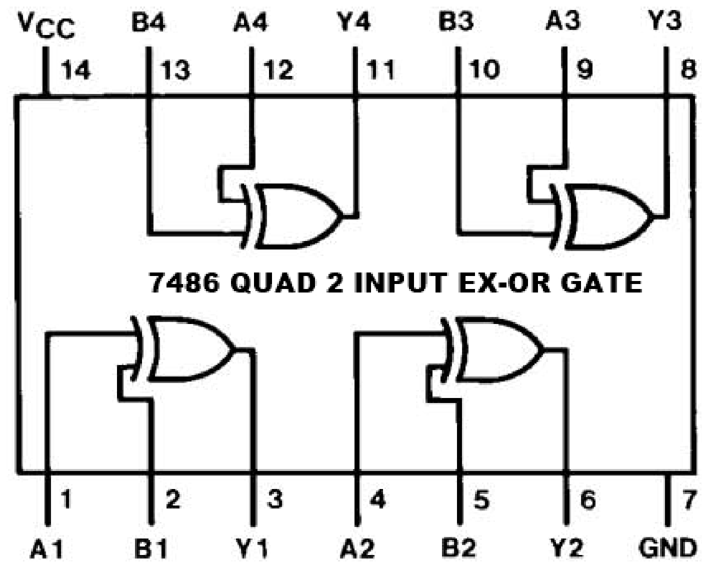




Extra: Implementing LFSRs in hardware

XOR gates





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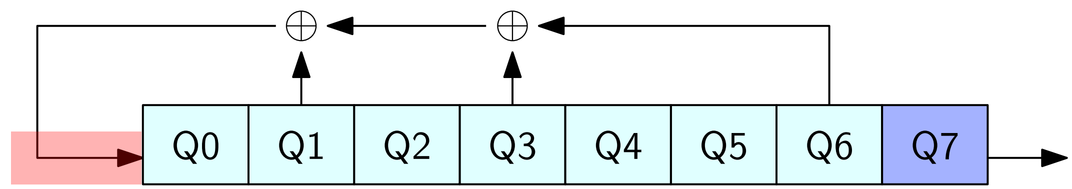

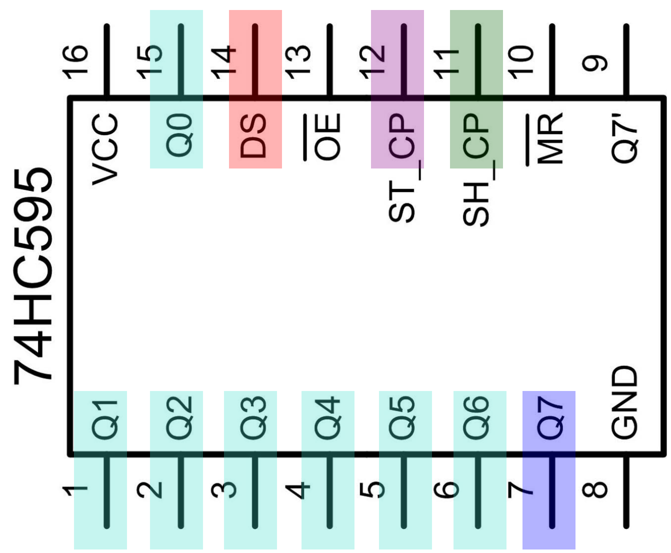

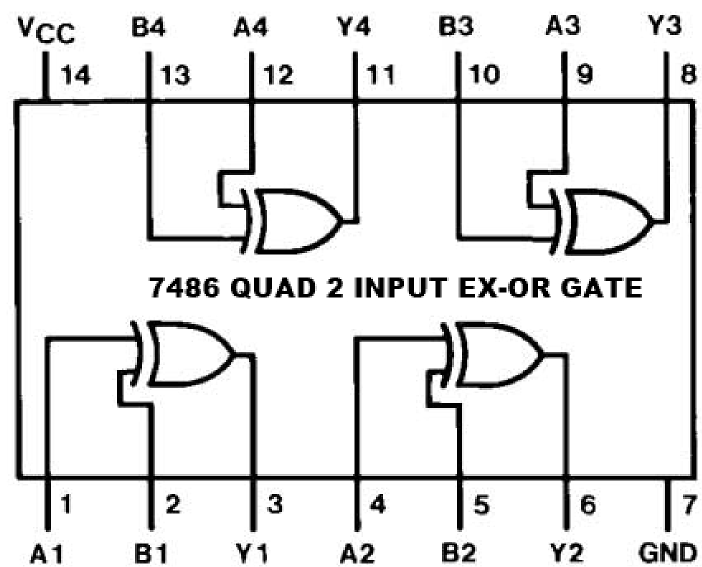

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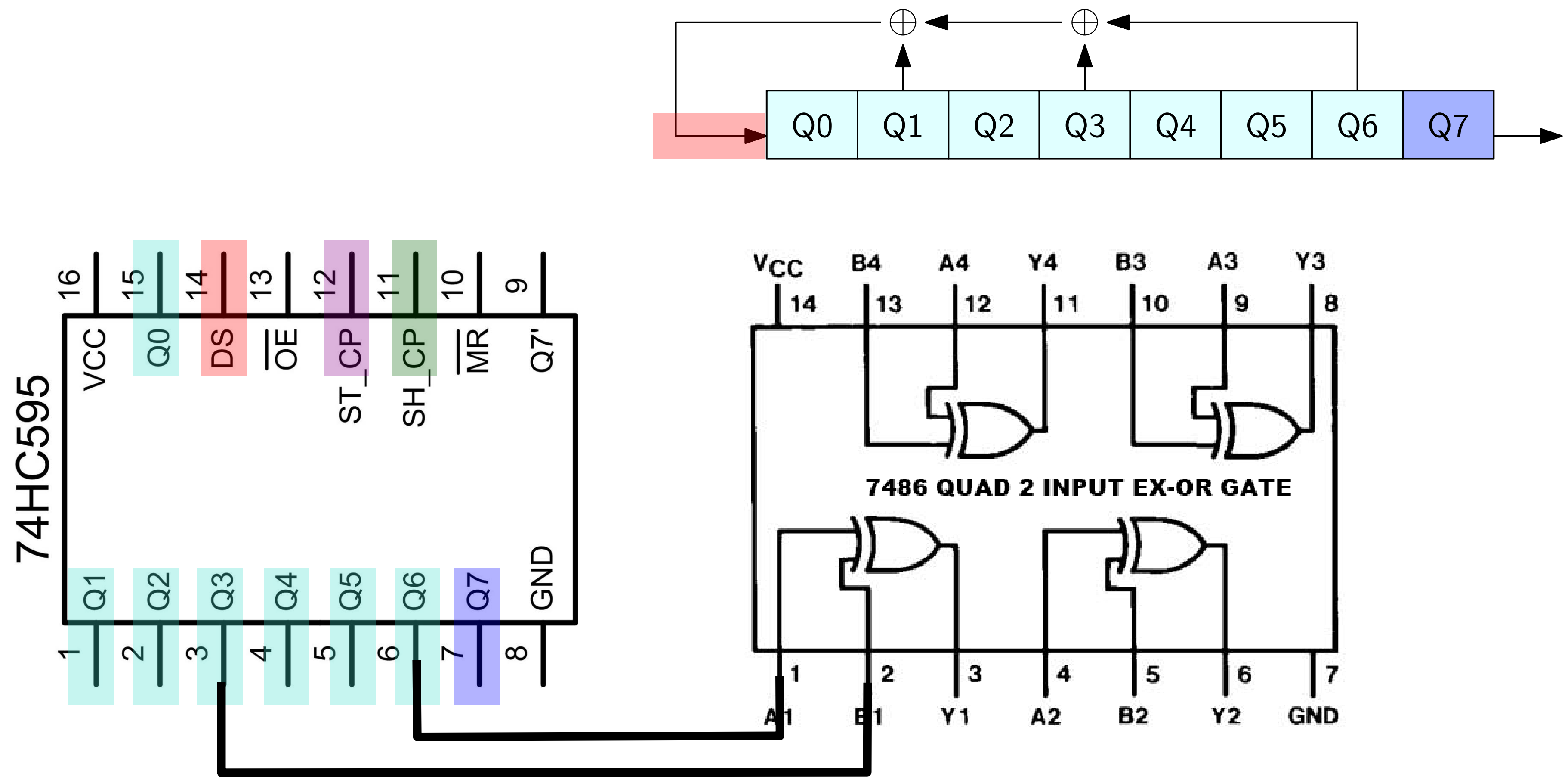

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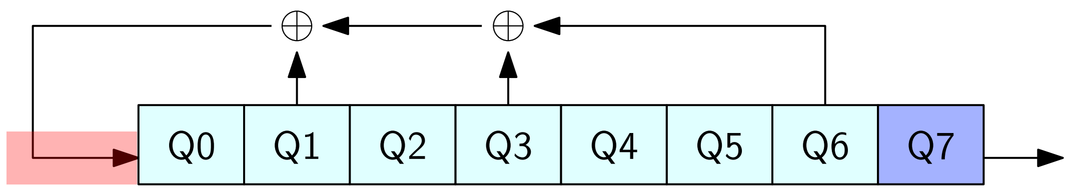

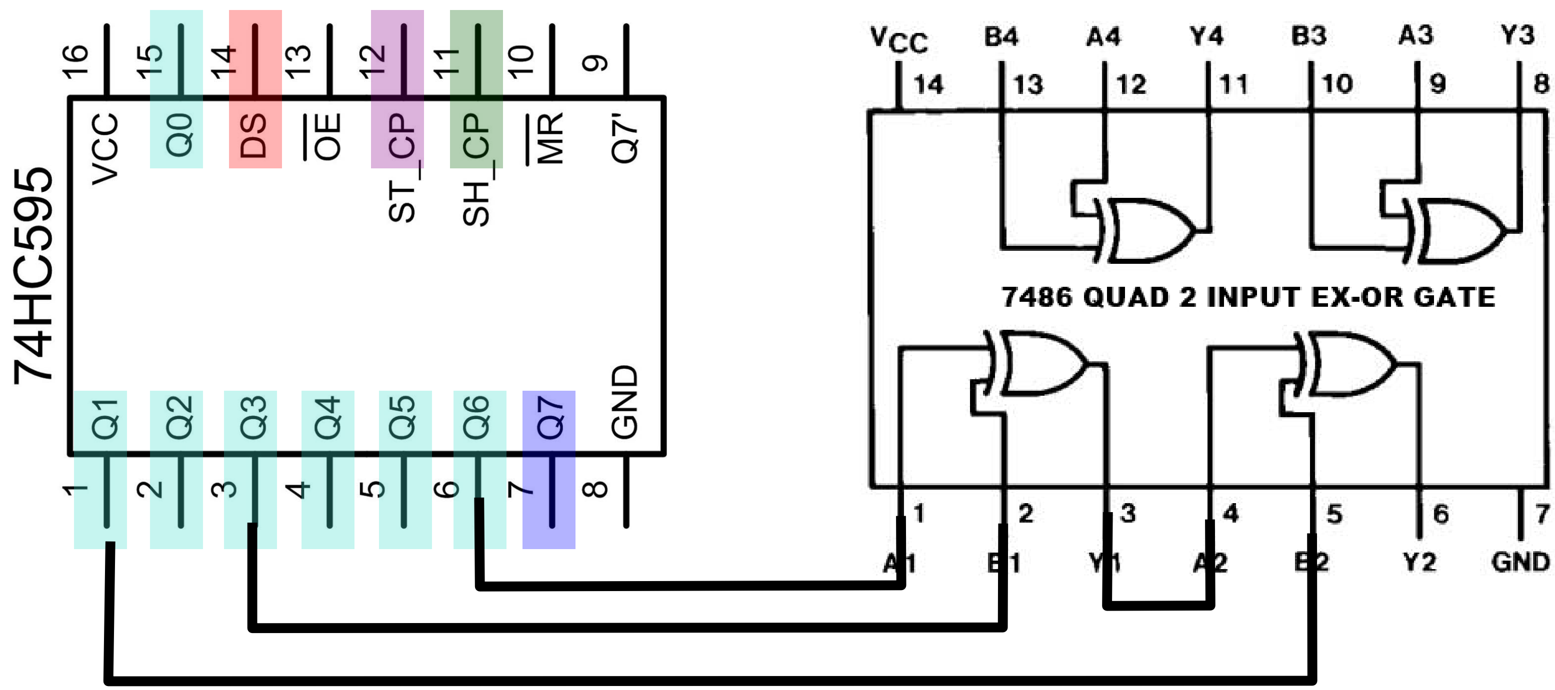

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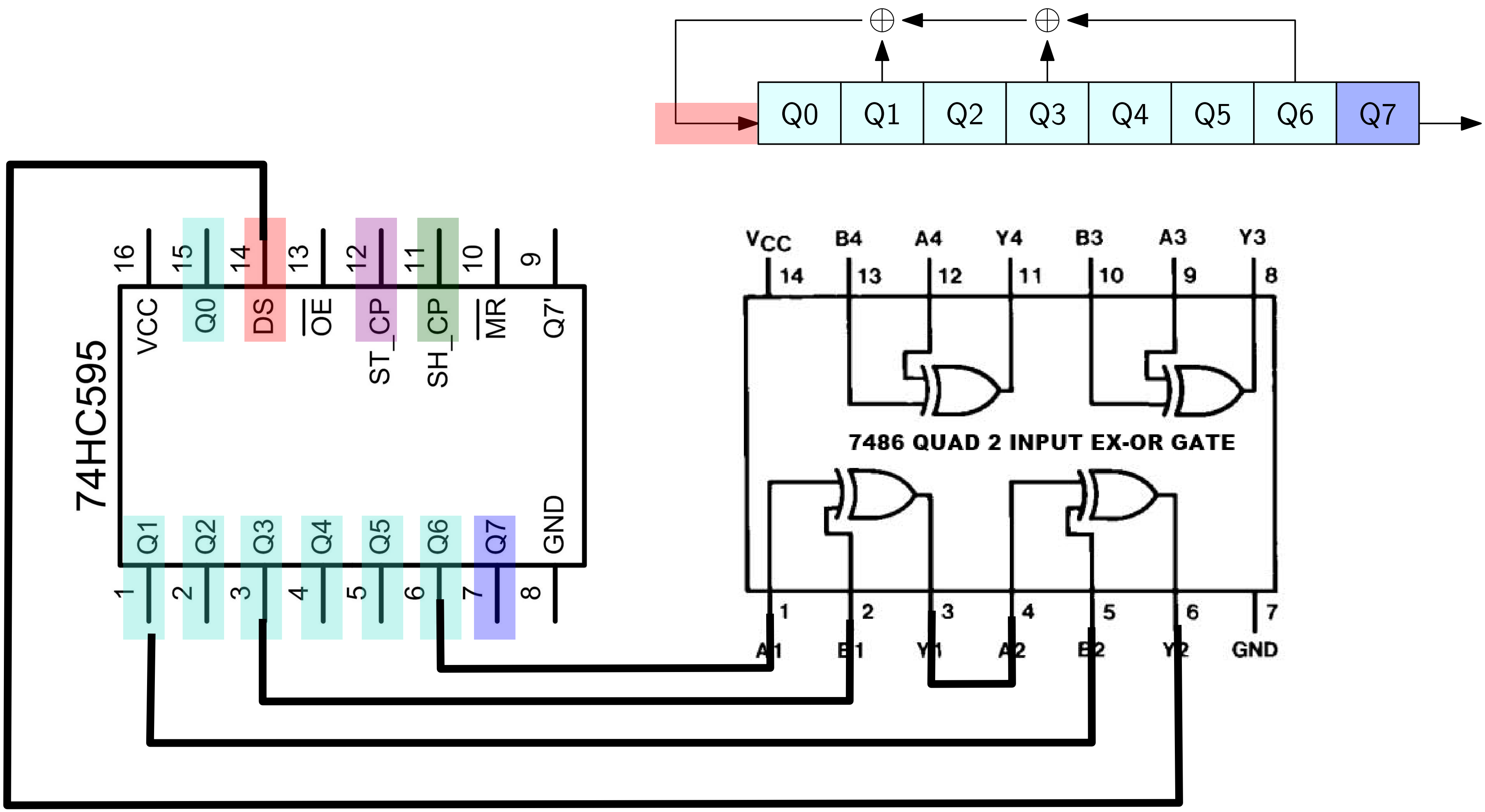

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